# RICOH  Li-ION/POLYMER 3/4-CELL PROTECTOR

## R5431Vxxxxx SERIES

## OUTLINE

The R5431Vxxxxx Series are high voltage CMOS-based protection ICs for over-charge/discharge of rechargeable three-cell/four-cell Lithium-ion (Li+) / Lithium polymer, further include a short circuit protection circuit for preventing large external short circuit current and the protection circuits against the excess discharge-current and excess charge current.

Each of these ICs is composed of eleven voltage detectors, a reference unit, a delay circuit, a short circuit protector, an oscillator, a counter, and a logic circuit. When the over-charge voltage threshold or excess-charge current threshold crosses the each detector threshold from a low value to a high value, the output of $C_{OUT}$ pin switches to "L" level after internal fixed delay time. To release over-charge detector after detecting over-charge, the detector can be reset and the output of $C_{OUT}$ becomes "H" when a kind of load is connected to $V_{DD}$ after a charger is disconnected from the battery pack and the cell voltage becomes lower than over-charge detector threshold. In case that a charger is continuously connected to the battery pack, if the cell voltage becomes lower than the over-charge detector threshold, over-charge state is also released.

The output of $D_{OUT}$ pin, the output of the over-discharge detector and the excess discharge-current detector, switches to "L" level after internally fixed delay time, when discharged voltage crosses the detector threshold from a high value to a value lower than $V_{DET2}$.

After detecting over-discharge voltage, when the cell voltage becomes higher than the released voltage from over-discharge, over-discharge state is released and the output of $D_{OUT}$ becomes "L".

By setting DS pin voltage as same as the VDD, the testing time of protection circuit board can be shortened. The delay time of the over-charge detector, over-discharge detector, and excess current detector can be reduced into approximately 1/50. The output type of $C_{OUT}$ and $D_{OUT}$ is CMOS.

# FEATURES

- Manufactured with High Voltage Tolerant Process ...Absolute Maximum Rating 30V
- Low supply current .................................Supply current (At normal mode) Typ. 12.0μA

    Standby current Typ. 6.0μA

- High accuracy detector threshold .............Over-charge detector (Ta=25°C) ±25mV

    Over-discharge detector ±2.5%

    Excess discharge-current detector ±20mV

    Excess charge-current detector ±30mV

- Variety of detector threshold

    Over-charge detector threshold 3.6V-4.5V step of 0.005V(VDET1n) (n=1,2,3,4)

    Over-discharge detector threshold 2.0V-3.0V step of 0.005V(VDET2n) (n=1,2,3,4)

    Excess discharge-current threshold1 VDD-0.20 V ( Fixed)

    Excess discharge-current threshold2 VDD-0.6V (Fixed)

    Short detector threshold VDD-1.2V (Fixed)

    Excess charge-current threshold VDD+0.2V ( Fixed)

    Over-charge released voltage VDET1n-0.1V to 0.4V step of 0.05V (VREL1n)

    (n=1,2,3,4)

    Over-discharge released voltage VDET2n+(0.2V to 0.7V, step of 0.1V) (VREL2n)

    (n=1,2,3,4)

- Internal fixed Output delay time...............Over-charge detector Output Delay 1.0s

    Over-discharge detector Output Delay 1.2s/128ms

    Excess discharge-current detector Output Delay 1 1.0s/12ms

    Excess discharge-current detector Output Delay2 10ms/2ms

    Excess charge-current detector Output Delay 8ms

    Short Circuit detector Output Delay 300μs

- Output Delay Time Shortening Function..By forcing VDD voltage level to DS pin, the Output Delay
    time of detect and release the over-charge/discharge, the
    excess-charge/discharge current can be reduced.
    If DS pin is not necessary, set the level to VSS. Especially,
    the Delay Time for over-charge/discharge, excess dis-
    charge current output delay 1 become about 1/50 of
    normal state.)

- 0V-battery charge...................................For each cell, charge inhibit voltage is set at Max.=1.1V.
    (Vnochgn, n=1,2,3,4)

- Small package .......................................SSOP-16

# APPLICATIONS

- Li+ ／ Li Polymer protector of over-charge, over-discharge, excess-current for battery pack
- Over-charge, discharge, and current protectors for notebook-PCs, power tools, and any other gadgets using on board Li+ ／ Li Polymer battery

# BLOCK DIAGRAMS
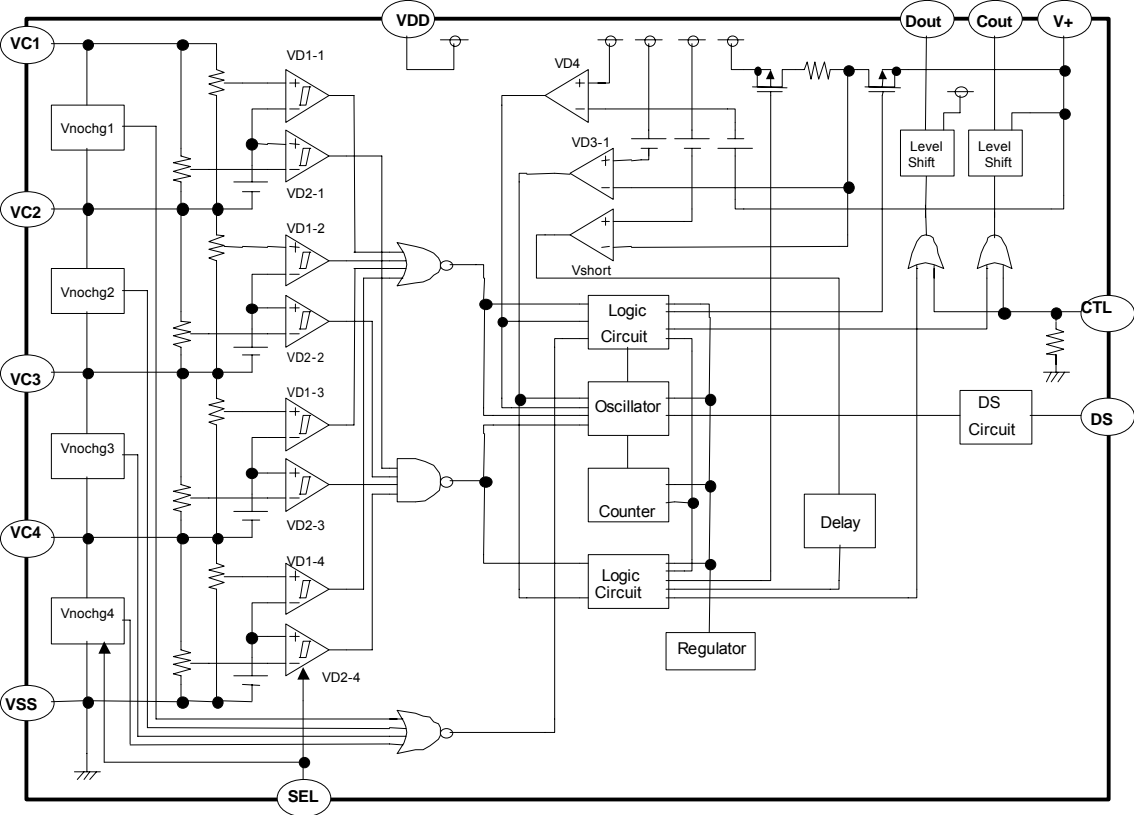
# SELECTION GUIDE

In the R5431Vxxxxx Series, input threshold of over-charge, over-discharge, excess charge/discharge current, and output delay time can be designated according to the application.

Part Number is designated as follows:

(ex.)

R5431V 301AA     ←Part Number

   ↑ ↑ ↑↑

   a   b   c d

| Code | Contents |
|------|----------|
| a | Package Type    V: SSOP-16 |
| b | Serial Number for the R5431 Series designating input threshold for over-charge, over-discharge, excess charge/discharge-current detectors. |
| c | Designation of Output delay option |
| d | Designation of version symbols. |

**\*Function Table**

| Code | Over-charge Released condition | Over-discharge Released condition | 0V battery charge inhibit |
|------|-------------------------------|----------------------------------|---------------------------|
| R5431VxxxAA | By voltage | By voltage | inhibit |
| R5431VxxxBA | By voltage | By voltage | inhibit |

| Code | Over-charge detector output delay time $t_{Vdet1}$ (ms) | Over-discharge detector output delay time $t_{Vdet2}$ (ms) | Excess-discharge current detector threshold output delay time 1 $t_{Vdet3-1}$(ms) | Excess-discharge current detector threshold output delay time 2 $t_{Vdet3-2}$ (ms) | Excess-charge current detector threshold output delay time $t_{Vdet4}$ (ms) | Short detector threshold output delay time $T_{short}(\mu s)$ |
|------|------|------|------|------|------|------|
| R5431VxxxAA | 1000 | 1200 | 1000 | 10 | 8 | 300 |
| R5431VxxxBA | 1000 | 128 | 12 | 2 | 8 | 300 |

**\*Product name list**

| Code | Over-charge detector threshold VDET1n (V) \*1 | Over-charge Released voltage VREL1n (V) \*1 | Over-discharge detector threshold VDET2n (V) \*1 | Over-discharge Released volt-ageVREL2n (V) \*1 | Excess-discharge Current detector threshold 1 VDET3-1 (V) \*2 | Excess-discharge current detector threshold 2 VDET3-2 (V) \*2 | Excess-charge current de-tector thresh-old VDET4 (V) \*2 |
|---|---|---|---|---|---|---|---|
| R5431V301AA | 4.350 | 4.150 | 2.300 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V303AA | 3.650 | 3.400 | 2.000 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V304AA | 4.300 | 4.100 | 2.300 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V301BA | 4.350 | 4.150 | 2.300 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V303BA | 3.650 | 3.400 | 2.000 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V304BA | 4.300 | 4.100 | 2.300 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V305BA | 3.900 | 3.700 | 2.500 | 2.800 | -0.200 | -0.600 | 0.200 |
| R5431V306BA | 4.275 | 4.075 | 2.700 | 3.000 | -0.200 | -0.600 | 0.200 |
| R5431V307BA | 4.275 | 4.075 | 2.300 | 2.700 | -0.200 | -0.600 | 0.200 |

**\*1: n=1,2,3,4**

**\*2: With reference to the $V_{DD}$ level**

# PIN CONFIGURATIONS

**SSOP-16**
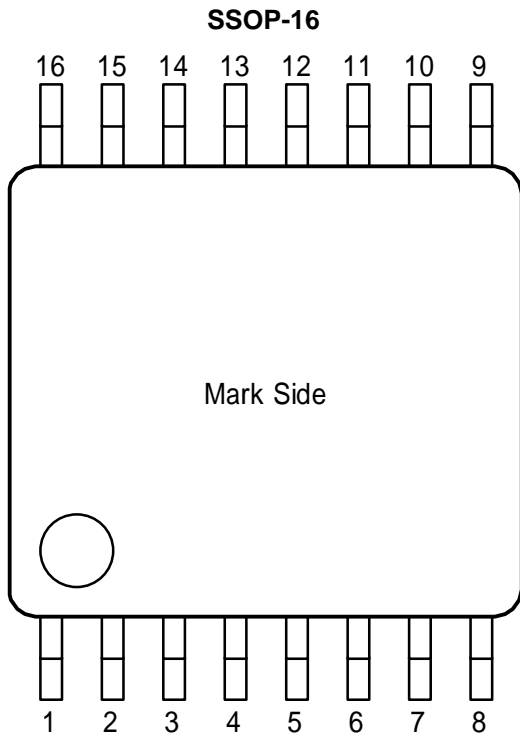


# PIN DESCRIPTION

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | $C_{OUT}$ | Output pin of over-charge detection, CMOS output |
| 2 | V+ | Charger positive terminal input pin |
| 3 | $D_{OUT}$ | Output pin of over-discharge detection, CMOS output |
| 4 | NC | No Connection |
| 5 | NC | No Connection |
| 6 | DS | Output Delay Time Shortening Pin |
| 7 | $V_{SS}$ | Vss pin. Ground pin for the IC |
| 8 | NC | No Connection |
| 9 | NC | No Connection |
| 10 | SEL | 3-cell/4-cell alternative pin |
| 11 | CTL | Charge/discharge FET control pin |
| 12 | $V_{C4}$ | Positive terminal Pin for Cell-4 |
| 13 | $V_{C3}$ | Positive terminal Pin for Cell-3 |
| 14 | $V_{C2}$ | Positive terminal pin for Cell-2 |
| 15 | $V_{C1}$ | Positive terminal pin for Cell-1 |
| 16 | $V_{DD}$ | $V_{DD}$ Pin |

# ABSOLUTE MAXIMUM RATINGS

Ta=25°C, Vss=0V

| Symbol | Item | Ratings | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 26 | V |
| $V_{C1}$ $V_{C2}$ $V_{C3}$ $V_{C4}$ $V+$ SEL CTL DS | Input Voltage Positive input pin for Cell-1 Positive input pin for Cell-2 Positive input pin for Cell-3 Positive input pin for Cell-4 Charger positive input pin voltage SEL pin voltage CTL pin voltage DS pin voltage | $V_{C2}$ -0.3 to $V_{C2}$+6.5 $V_{C3}$ –0.3 to $V_{C3}$+6.5 $V_{C4}$ –0.3 to $V_{C4}$+6.5 Vss-0.3 to Vss+6.5 Vss-0.3 to 30 Vss-0.3 to $V_{DD}$+0.3 Vss-0.3 to $V_{DD}$+0.3 Vss-0.3 to $V_{DD}$+0.3 | V |
| $VC_{OUT}$ $VD_{OUT}$ | Output voltage $C_{OUT}$ pin $D_{OUT}$ pin | $V_{ss}$ –0.3 to 30 $V_{ss}$ -0.3 to $V_{DD}$ +0.3 | V V |
| $P_D$ | Power dissipation | 685 | mW |
| Ta | Operating temperature range | -40 to 85 | °C |
| Tstg | Storage temperature range | -55 to 125 | °C |

# ELECTRICAL CHARACTERISTICS

R5431V3XXAA                                     Unless otherwise specified, Ta=25°C

| Symbol | Item | Conditions | Min. | Typ. | Max. | Unit |
|--------|------|-----------|------|------|------|------|
| $V_{DD1}$ | Operating input voltage | Voltage defined as $V_{DD}$-$V_{SS}$ | 2 | | 20 | V |
| Vnochgn | Maximum charge inhibit Voltage (n=1,2,3,4) | $V_{DD}=V_{C1}$ $V_{DD}=V+$ | | | 1.100 | V |
| $V_{DET1n}$ | CELLn Over-charge threshold (n=1,2,3,4) | Detect rising edge of supply voltage Rn=330Ω | $V_{DET1n}$-0.025 | $V_{DET1n}$ | $V_{DET1n}$+0.025 | V |
| $V_{REL1n}$ | CELLn Over-charge released voltage | Rn=330Ω | $V_{REL1n}$-0.050 | $V_{REL1n}$ | $V_{REL1n}$+0.050 | V |
| $tV_{DET1}$ | Output delay of over-charge | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=3.5V to 4.5V (n=2,3,4) | 0.7 | 1.0 | 1.3 | s |
| $tV_{REL1}$ | Output delay of release from over-charge | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=4.5V to 3.5V (n=2,3,4) | 11 | 16 | 21 | ms |
| $V_{DET2n}$ | CELLn Over-discharge threshold (n=1,2,3,4) | Detect falling edge of supply voltage | $V_{DET2n}$×0.975 | $V_{DET2n}$ | $V_{DET20}$×1.025 | V |
| $V_{REL2n}$ | CELLn Released Voltage from Over-discharge (n=1,2,3,4) | Detect rising edge of supply voltage | $V_{REL2n}$×0.975 | $V_{REL2n}$ | $V_{REL2n}$×1.025 | V |
| $tV_{DET2}$ | Output delay of over-discharge | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=3.5V to 2.0V (n=2,3,4) | 0.8 | 1.2 | 1.6 | s |
| $tV_{REL2}$ | Output delay of release from over-discharge | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=2.0V to 3.5V, (n=2.3.4) | 0.7 | 1.2 | 1.7 | ms |
| $V_{DET3-1}$ | Excess discharge-current threshold 1 | Detect falling edge, VDD pin voltage base | $V_{DET3}$-0.020 | $V_{DET3-1}$ | $V_{DET3-1}$ +0.020 | V |
| $V_{DET3-2}$ | Excess discharge-current threshold 2 | Detect falling edge, VDD pin voltage base | -0.700 | -0.600 | -0.500 | V |
| $tV_{DET3-1}$ | Output delay of excess discharge current 1 | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$ to $V_{DET3-1}$-0.1V, (n=1,2,3,4) | 0.7 | 1.0 | 1.3 | s |
| $tV_{DET3-2}$ | Output delay of excess discharge current 2 | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$ to $V_{DET3-2}$-0.2V, (n=1,2,3,4) | 7 | 10 | 13 | ms |
| $tV_{REL3}$ | Output delay of release from excess discharge-current | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DET3-2}$-0.1V to $V_{DD}$ (n=1,2,3,4) | 0.7 | 1.2 | 1.7 | ms |
| $V_{DET4}$ | Excess charge-current threshold | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V (n=1,2,3,4) Detect rising edge, the value is $V_{DD}$ base. | 0.17 | 0.20 | 0.23 | V |
| $tV_{DET4}$ | Output delay of excess charge-current | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, V+=VDD to VDD+0.5V, (n=1,2,3,4) VDD base | 5 | 8 | 11 | ms |
| $tV_{REL4}$ | Output delay of release from excess charge-current | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$+0.5V to $V_{DD}$ (n-1,2,3,4) | 0.7 | 1.2 | 1.7 | ms |
| Vshort | Short protection voltage | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, $V_{DD}$ base (n=1,2,3,4) | -1.7 | -1.2 | -0.7 | V |
| tshort | Output Delay of Short protection | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$ to $V_{DD}$+0.5V, (n=1,2,3,4) | 200 | 300 | 500 | μs |
| Rshort | Reset resistance for Excess Discharge current protection | $V_{DD}$=14.4V, V+=VDD-1V | 15 | 30 | 65 | kΩ |
| Iss | Supply current | $V_{DD}=V_{C1}$, $V_{CELLn}$=3.9V (n=1,2,3,4) | | 12 | 30 | μA |
| $I_{stb}$ | Standby current | $V_{DD}=V_{C1}$, $V_{CELLn}$=2.0V (n=1,2,3,4) | | 6 | 12 | μA |

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4

R5431V3XXBA version                                    Unless otherwise specified, Ta=25°C

| Symbol | Item | Conditions | Min. | Typ. | Max. | Unit |
|--------|------|-----------|------|------|------|------|
| $V_{DD1}$ | Operating input voltage | Voltage defined as $V_{DD}$-$V_{SS}$ | 2 | | 20 | V |
| Vnochgn | Maximum charge inhibit Voltage (n=1,2,3,4) | $V_{DD}$=$V_{C1}$ $V_{DD}$=V+ | | | 1.100 | V |
| $V_{DET1n}$ | CELLn Over-charge threshold (n=1,2,3,4) | Detect rising edge of supply voltage Rn=330Ω | $V_{DET1n}$-0.025 | $V_{DET1n}$ | $V_{DET1n}$+0.025 | V |
| $V_{REL1n}$ | CELLn Over-charge released voltage | Rn=330Ω | $V_{REL1n}$-0.050 | $V_{REL1U}$ | $V_{REL1n}$+0.050 | V |
| $tV_{DET1}$ | Output delay of over-charge | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=3.5V to 4.5V (n=2,3,4) | 0.7 | 1.0 | 1.3 | s |
| $tV_{REL1}$ | Output delay of release from over-charge | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=4.5V to 3.5V (n=2,3,4) | 11 | 16 | 21 | ms |
| $V_{DET2n}$ | CELLn Over-discharge threshold (n=1,2,3,4) | Detect falling edge of supply voltage | $V_{DET2n}$×0.975 | $V_{DET2n}$ | $V_{DET20}$×1.025 | V |
| $V_{REL2n}$ | CELLn Released Voltage from Over-discharge (n=1,2,3,4) | Detect rising edge of supply voltage | $V_{REL2n}$×0.975 | $V_{REL2n}$ | $V_{REL2n}$×1.025 | V |
| $tV_{DET2}$ | Output delay of over-discharge | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=3.5V to 2.0V (n=2,3,4) | 89 | 128 | 167 | ms |
| $tV_{REL2}$ | Output delay of release from over-discharge | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, $V_{CELL1}$=2.0V to 3.5V, (n=2.3.4) | 0.7 | 1.2 | 1.7 | ms |
| $V_{DET3-1}$ | Excess discharge-current threshold 1 | Detect falling edge, VDD voltage base | $V_{DET3-1}$-0.020 | $V_{DET3-1}$ | $V_{DET3-1}$ +0.020 | V |
| $V_{DET3-2}$ | Excess discharge-current threshold 2 | Detect falling edge, VDD voltage base | -0.700 | -0.600 | -0.500 | V |
| $tV_{DET3-1}$ | Output delay of excess discharge current 1 | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$ to $V_{DET3-1}$-0.1V, (n=1,2,3,4) | 8 | 12 | 16 | ms |
| $tV_{DET3-2}$ | Output delay of excess discharge current 2 | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$ to $V_{DET3-2}$-0.2V, (n=1,2,3,4) | 1.4 | 2.0 | 2.6 | ms |
| $tV_{REL3}$ | Output delay of release from excess discharge-current | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DET3-2}$-0.1V to $V_{DD}$ (n=1,2,3,4) | 0.7 | 1.2 | 1.7 | ms |
| $V_{DET4}$ | Excess charge-current threshold | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V (n=1,2,3,4) Detect rising edge, the value is $V_{DD}$ base. | 0.17 | 0.20 | 0.23 | V |
| $tV_{DET4}$ | Output delay of excess charge-current | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, V+=VDD to VDD+0.5V, (n=1,2,3,4) VDD base | 5 | 8 | 11 | ms |
| $tV_{REL4}$ | Output delay of release from excess charge-current | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$+0.5V to $V_{DD}$ (n-1,2,3,4) | 0.7 | 1.2 | 1.7 | ms |
| Vshort | Short protection voltage | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, $V_{DD}$ base (n=1,2,3,4) | -1.7 | -1.2 | -0.7 | V |
| tshort | Output Delay of Short protection | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.5V, V+=$V_{DD}$ to $V_{DD}$+0.5V, (n=1,2,3,4) | 200 | 300 | 500 | μs |
| Rshort | Reset resistance for Excess Discharge current protection | $V_{DD}$=14.4V, V+=$V_{DD}$-1V | 15 | 30 | 65 | kΩ |
| $I_{SS}$ | Supply current | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=3.9V (n=1,2,3,4) | | 12 | 30 | μA |
| $I_{Stb}$ | Standby current | $V_{DD}$=$V_{C1}$, $V_{CELLn}$=2.0V (n=1,2,3,4) | | 6 | 12 | μA |

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4

Input／Output Pins (R5431V3XXAA／BA common)          Unless otherwise specified, Ta=25°C

| Symbol | Item | Conditions | Min. | Typ. | Max. | Unit |
|--------|------|------------|------|------|------|------|
| $V_{IH1}$ | SEL pin "H" input voltage | | $V_{DD}$ x 0.8 | | $V_{DD}$ +0.3 | V |
| $V_{IL1}$ | SEL pin "L" input voltage | | $V_{SS}$-0.3 | | $V_{DD}$ x 0.2 | V |
| $V_{IH2}$ | CTL pin "H" input voltage | | $V_{DD}$ x 0.8 | | $V_{DD}$+0.3 | V |
| $V_{IL2}$ | CTL pin "L" input voltage | | $V_{SS}$-0.3 | | $V_{DD}$ x 0.2 | V |
| $V_{IH3}$ | DS pin "H" input voltage | | $V_{DD}$ x 0.8 | | $V_{DD}$+0.3 | V |
| $V_{IL3}$ | DS pin "L" input voltage | | $V_{SS}$-0.3 | | $V_{DD}$ x 0.2 | ms |
| $V_{OL1}$ | $C_{OUT}$ Nch ON voltage | $I_{OL}$=50μA, $V_{DD}$=$V_{C1}$, Vcelln=3.5V (n=1,2,3,4), CTL=Vss | | 0.1 | 0.5 | V |
| $V_{OH1}$ | $C_{OUT}$ Pch ON voltage | $I_{OH}$=-50μA, $V_{DD}$=$V_{C1}$, Vcelln=3.5V (n=1,2,3,4), CTL=$V_{DD}$ | 13.5 | 13.9 | | V |
| $V_{OL2}$ | $D_{OUT}$ Nch ON voltage | $I_{OL}$=50μA, $V_{DD}$=$V_{C1}$, Vcelln=3.5V (n=1,2,3,4), CTL=Vss | | 0.1 | 0.5 | V |
| $V_{OH2}$ | $D_{OUT}$ Pch ON voltage | $I_{OH}$=-50μA, $V_{DD}$=$V_{C1}$, Vcelln=3.5V (n=1,2,3,4), CTL=$V_{DD}$ | 13.5 | 13.9 | | V |
| $I_{IH}$ | CTL pin "H" input current | $V_{DD}$=VC1, $V_{CELLn}$=3.5V, (n=1,2,3,4), CTL=14V | 0.15 | 0.70 | 1.60 | μA |

# OPERATION

- **VDET1n / Over-Charge Detectors (n=1, 2, 3, 4)**

While the cell is charged, the voltage between VC1 pin and VC2 pin (the voltage of the Cell-1), the voltage between VC2 pin and VC3 pin (the voltage of the Cell-2), the voltage between VC3 pin and VC4 pin (the voltage of the Cell-3), the voltage of VC4 pin and VSS pin (the voltage of Cell-4) are supervised. Even if one of the cells' voltage becomes equal or more than the over-charge detector threshold, the over-charge is detected, and an external charge control Pch MOSFET turns off with C$_{OUT}$ pin being at "H" level.

To reset the over-charge and make the C$_{OUT}$ pin level to "L" again after detecting over-charge, in such conditions that a time when the all Cells' voltages are down to a level lower than over-charge voltage, by connecting a kind of load to V$_{DD}$ after disconnecting a charger from the battery pack. Then, the output voltage of C$_{OUT}$ pin becomes "L", and it makes an external Pch MOSFET turn on, and charge cycle is available. If a charger is continuously connected to the battery pack, when all the cells voltages are lower than the released voltage from over-charge, charge cycle is acceptable. Thus, this over-charge detector has hysteresis. To judge whether or not load is connected, the built-in excess-discharge current detector is used. By connecting some load, V+ pin voltage becomes equal or less than excess-discharge current detector threshold, and reset the over-charge detecting state.

Further, even if when one of the cells is equal or higher than the over-charge detector threshold, if a charger is removed and some load is connected, COUT outputs "H", however, load current can flow through the parasitic diode of the external charge control Pch MOSFET. After that, when the V$_{DD}$ pin voltage becomes lower than the over-charge detector threshold, C$_{OUT}$ becomes "L".

Internal fixed output delay times for over-charge detection and release from over-charge exist. Even if one of voltage of Cells keeps its level more than the over-charge detector threshold, and output delay time passes, over-charge voltage is detected. Even when the voltage of each cell becomes equal or higher level than V$_{DET1}$ if these voltages would be back to a level lower than the over-charge detector threshold within a time period of the output delay time, the over-charge is not detected. Besides, after detecting over-charge, each Cell voltage is lower than the over-charge detector threshold, even if a charger is removed and a load is connected, if the voltage is recovered within output delay time of release from over-charge, over-charge state is not released.

A level shifter incorporated in a buffer driver for the C$_{OUT}$ pin makes the "H" level of C$_{OUT}$ pin to the V+ pin voltage.

The output of the C$_{OUT}$ pin is Vss and V+ with CMOS buffer.

- **VDET2n / Over-Discharge Detectors (n=1, 2, 3, 4)**

While the cells are discharged, the voltage between VC1 pin and VC2 pin (the voltage of Cell1) , the

voltage between VC2 pin and VC3 pin (Cell2 voltage), the voltage between VC3 pin and VC4 pin (Cell3 voltage) , and the voltage between VC4 pin and Vss pin (Cell4 voltage) are supervised. Even if one of the cells' voltage becomes equal or less than the over-discharge detector threshold, the over-discharge is detected and discharge stops by the external discharge control Pch MOSFET turning off with the D$_{OUT}$ pin being at "H" level.

The condition to release over-discharge voltage detector is that connecting a charger to the battery after detecting over-discharge voltage, and when the cell voltage becomes lower than over-discharge detector threshold, some charge current flows through the parasitic diode of an external Pch MOSFET, and when each cell voltage is higher than the released voltage from over-discharge, DOUT pin becomes "L" level, and by turning on the external Pch MOSFET, discharge becomes possible. When a charger is connected to the battery, if each cell is more than the released voltage from over-discharge, after the delay time of the released from over-discharge, DOUT pin becomes "L". Thus, the over-discharge detector has hysteresis.

The output delay time for over-discharge detect is fixed internally. Even if one of the voltage of Cells is down to equal or lower than the over-discharge detector threshold, if the voltage of each Cell would be back to a level higher than the over-discharge detector threshold within a time period of the output delay time, the over-discharge is not detected. Output delay time for release from over-discharge is also set.

After detecting over-discharge, supply current would be reduced and be into standby by halting unnecessary circuits and consumption current of the IC itself is made as small as possible.

When a cell voltage equals to zero, if the voltage of each cell is lower than charge inhibit maximum voltage, charge is not acceptable. All the cell voltages are higher than charge inhibit maximum voltage, C$_{OUT}$ pin becomes "L" and a system is allowable to charge.

The output type of D$_{OUT}$ pin is CMOS having "H" level of V$_{DD}$ and "L" level of V$_{SS}$.

- **VDET3-n (n=1, 2) /Excess discharge-current Detector, Short Circuit Protector**

When the charge and discharge is acceptable, V+ pin voltage is supervised, if the load is short and V+ pin voltage becomes equal or lower than excess discharge current threshold, and equal or more than short detector threshold, the status becomes excess discharge current detected condition. If V+ pin voltage becomes equal or lower than short circuit detector threshold, the status becomes short circuit detected, then DOUT pin outputs "H" and by turning off the external Pch MOSFET, large current flow is prevented. As for version A, excess discharge current detector has two thresholds, and each threshold has the output delay time. In terms of the output delay times, the delay time for the excess discharge current detector 2 is set shorter than excess discharge current 1.

The output delay times for the excess discharge-current detectors are internally fixed.

A quick recovery of V+ pin level from a value between Excess discharge current detector and short circuit detector threshold within the delay time, may keep the status as before excess discharge current detected. Output delay time for Release from excess discharge-current detection is also set. When the short circuit protector is enabled, the delay time is also set.

The V + pin has a built-in pull-down resistor to the Vss pin, that is, the resistance to release from excess-discharge current.

After an excess discharge-current or short circuit protection is detected, removing a cause of excess discharge-current or external short circuit and opened, V+ pin level is going to the VDD pin level, through the built-in pulled down resistor. When the V+ pin becomes equal or more than excess discharge current detector threshold, the excess-discharge current or short circuit status is automatically released. The reset resistor of excess discharge-current is off at normal state. Only when detecting excess discharge-current or short circuit, the resistor is on.

Output delay time of excess discharge-current is set shorter than the delay time for over-discharge detector. Therefore, if $V_{DD}$ voltage would be lower than $V_{DET2n}$ at the same time as the excess discharge-current is detected, the R5431Vxxxxx is at excess discharge-current detection mode. By disconnecting a load and opened, the excess discharge current status is automatically released.

- **VDET4/ Excess charge-current detector**

When the battery pack is chargeable and discharge is also possible, VDET4 senses V+ pin voltage. For example, in case that a battery pack is charged by an inappropriate charger, an excess current flows, then the voltage of V+ pin becomes equal or more than excess charge-current detector threshold, then the output of $C_{OUT}$ becomes "H", and prevents from flowing excess current in the circuit by turning off the external Pch MOSFET.

Output delay of excess charge current is internally fixed. Even the voltage level of V+ pin becomes equal or lower than the excess charge-current detector threshold, if the voltage becomes lower than excess charge current threshold within the delay time, the excess charge current is not detected. Output delay for the release from excess charge current is also set.

VDET4 can be released with disconnecting a charger and connecting a load.

- **DS (Delay Shorten) function**

Output delay time of over-charge, over-discharge, excess discharge current, excess charge current and release from those detecting modes can be shorter than those setting value by forcing VDD voltage level to DS pin.

- **Operation against cell Unbalance**

If one of the cells detects over-charge and the output of $C_{OUT}$ becomes "H", even if the other cell detects over-discharge, the over-charge status is maintained and the output of $C_{OUT}$ keeps "H". If one of the cell detects over-charge and the output of $C_{OUT}$ becomes "H", the other cell detects

over-discharge and the former cell is released from over-charge, after the delay time of the released from over-charge, the output of COUT becomes "L", and after the delay time of detecting over-discharge, the output of DOUT becomes "H". After detecting over-discharge, internal unnecessary circuits are halted and the R5431V is into the standby mode. (Supply current Typ. 6.0μA)

- **Charge inhibit detector Vnochg-n (n=1, 2, 3, 4)**

  Charge inhibit detector is equipped for each cell. Even if one of the cells' voltage is equal or lower than charge inhibit voltage, when a charger is connected, charge inhibit is detected, the output of COUT becomes "H", then by turning off the external Pch MOSFET, the charge is halted.

  While the charge inhibit status, the cell voltage with equal or lower than the charge inhibit voltage is equal or lower than over-discharge voltage, both of the outputs of COUT and DOUT become "H" and the external MOSFETS become "off"/"off". Other than charge inhibit status, external MOSFETs will never be "off"/"off".

- **CTL pin**

  By forcing VDD voltage level to CTL pin, the outputs of COUT and DOUT are set "H" compulsory.

  CTL pin input and outputs of COUT and DOUT

  | CTL pin input | $C_{OUT}$ output | $D_{OUT}$ output |
  | --- | --- | --- |
  | High | High | High |
  | Open | normal | normal |
  | Low | normal | normal |

- **SEL pin**

  SEL pin is used as switch over 3-cell protector and 4-cell protector. By forcing VSS voltage level to SEL pin, the operation of 4th cell's protection circuit, the signal is shut down, therefore, even if the 4th cell is shortened, over-discharge is not detected and operates as a 3-cell protector IC.

  SEL pin must be set as $V_{DD}$ voltage or $V_{SS}$ voltage level.

  SEL pin input and operation mode

  | SEL pin input | Operation Mode |
  | --- | --- |
  | High | 4-cell protector |
  | Open | Indefinite |
  | Low | 3-cell protector |

# TIMING CHART

(1) Timing diagram of Over-charge, Excess charge current
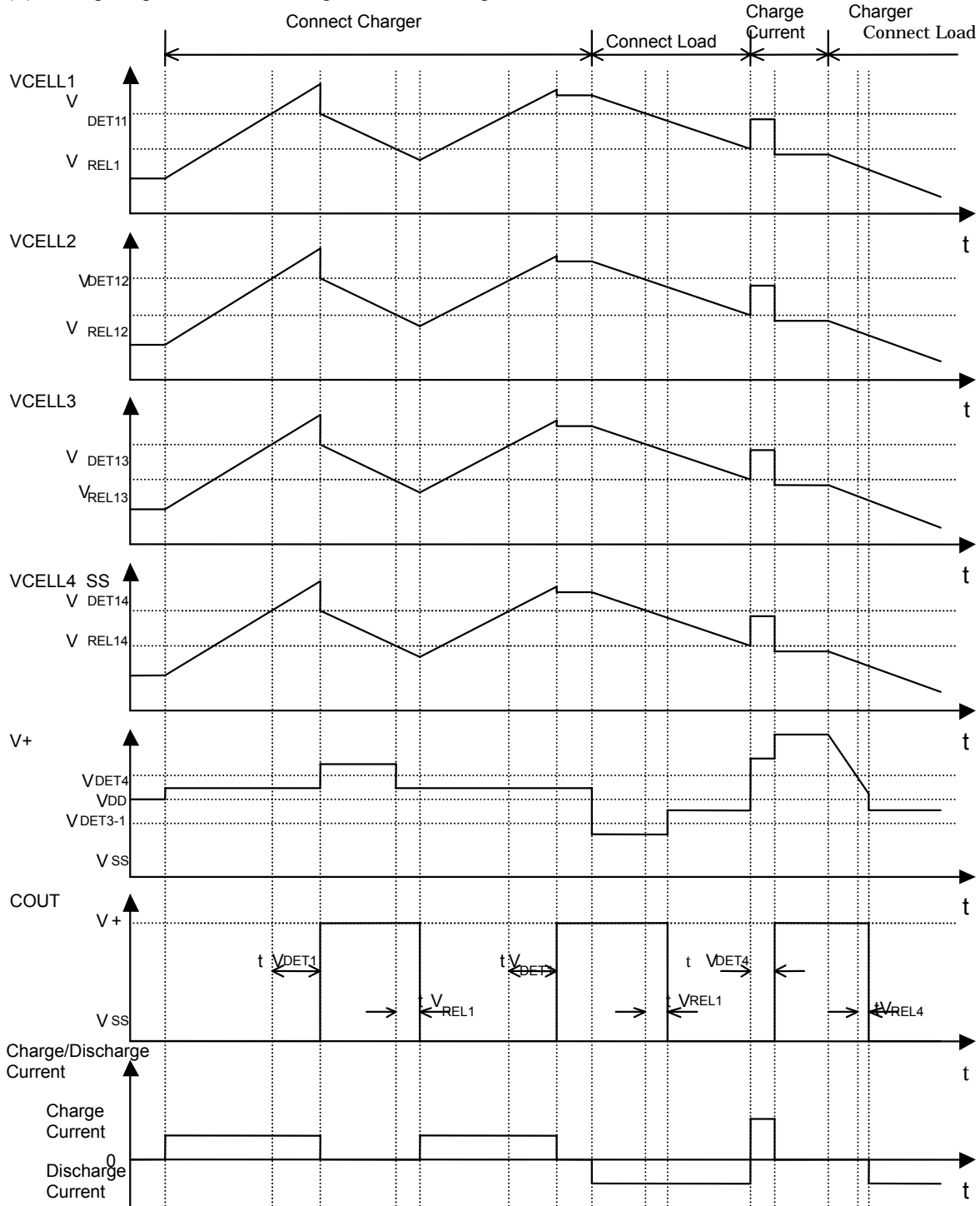
(2) Over-discharge, Excess discharge current1, 2, Short circuit
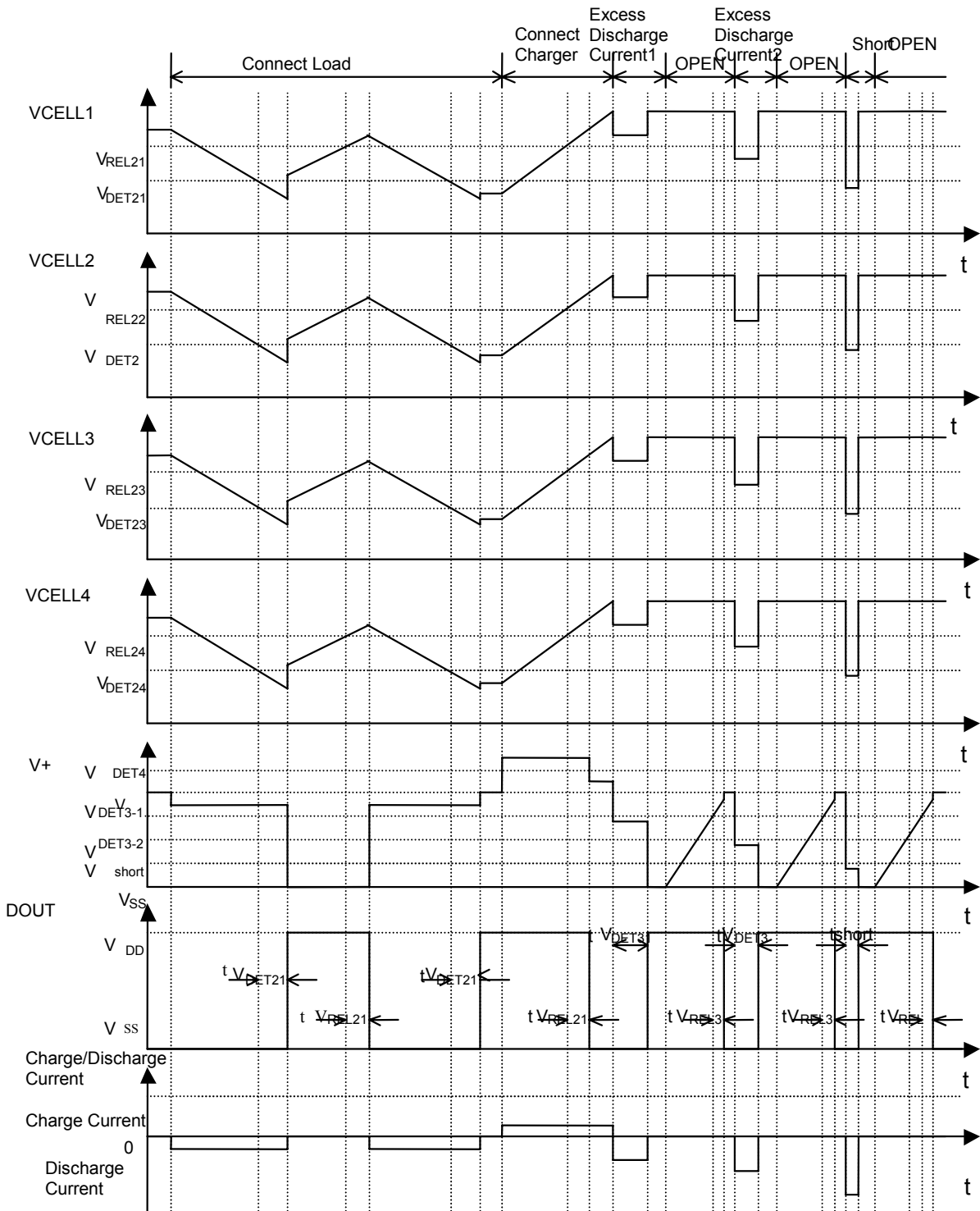
# TYPICAL APPLICATION AND TECHNICAL NOTES

*Circuit example (for 4-cell protection)
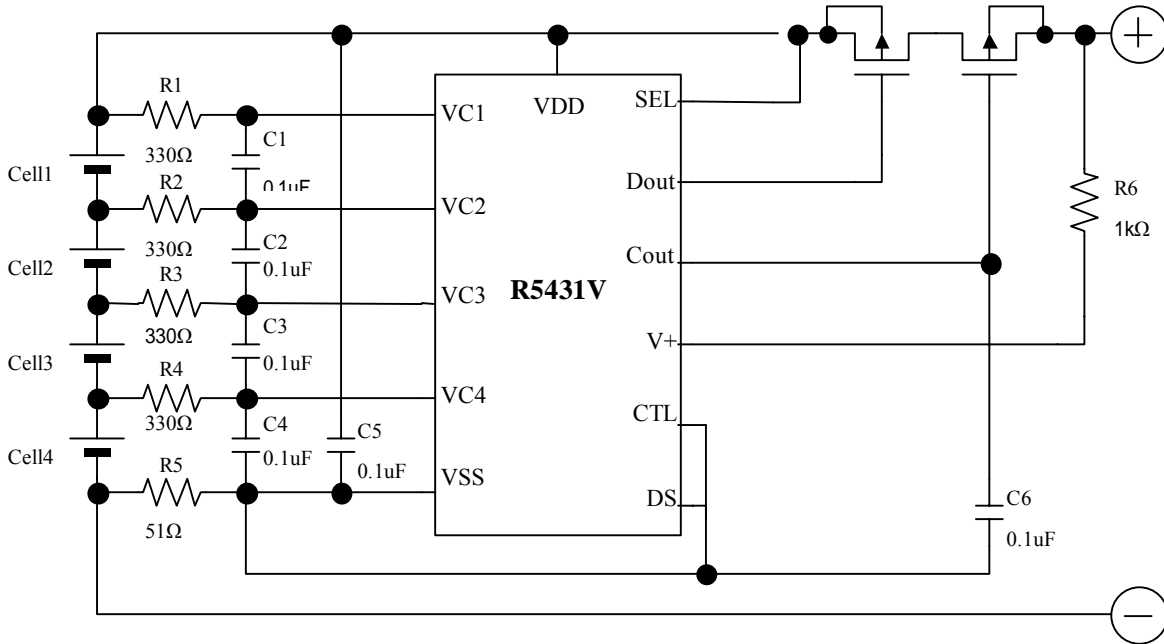


* Circuit example (for 3-cell protection)
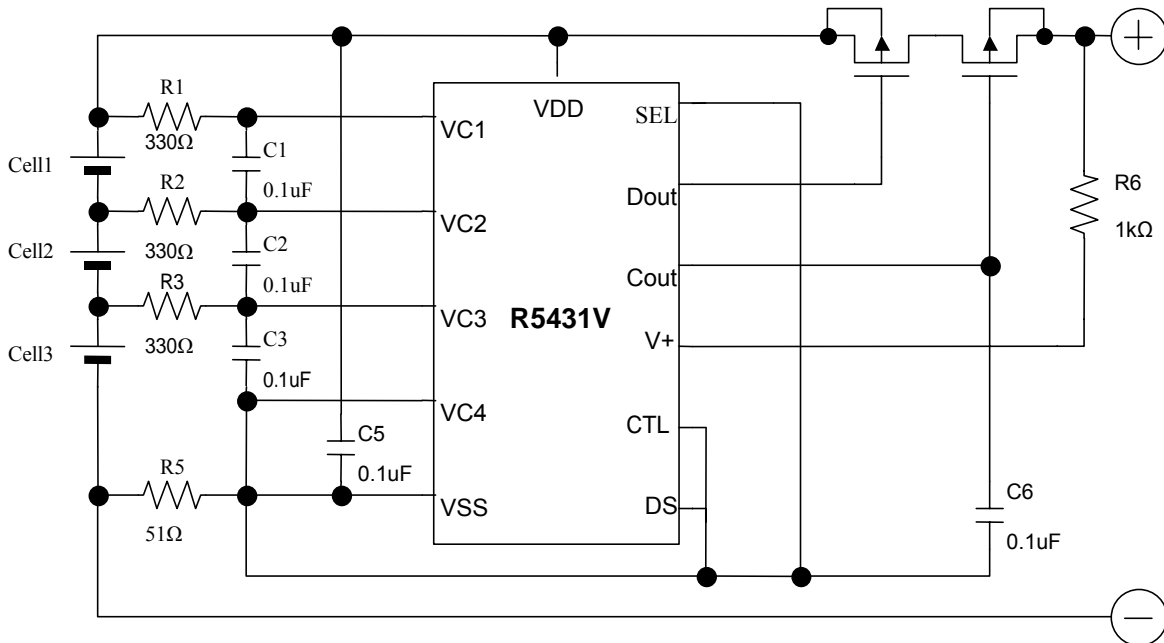
*Circuit example (for 4-cell protection with CTL function and DS function)
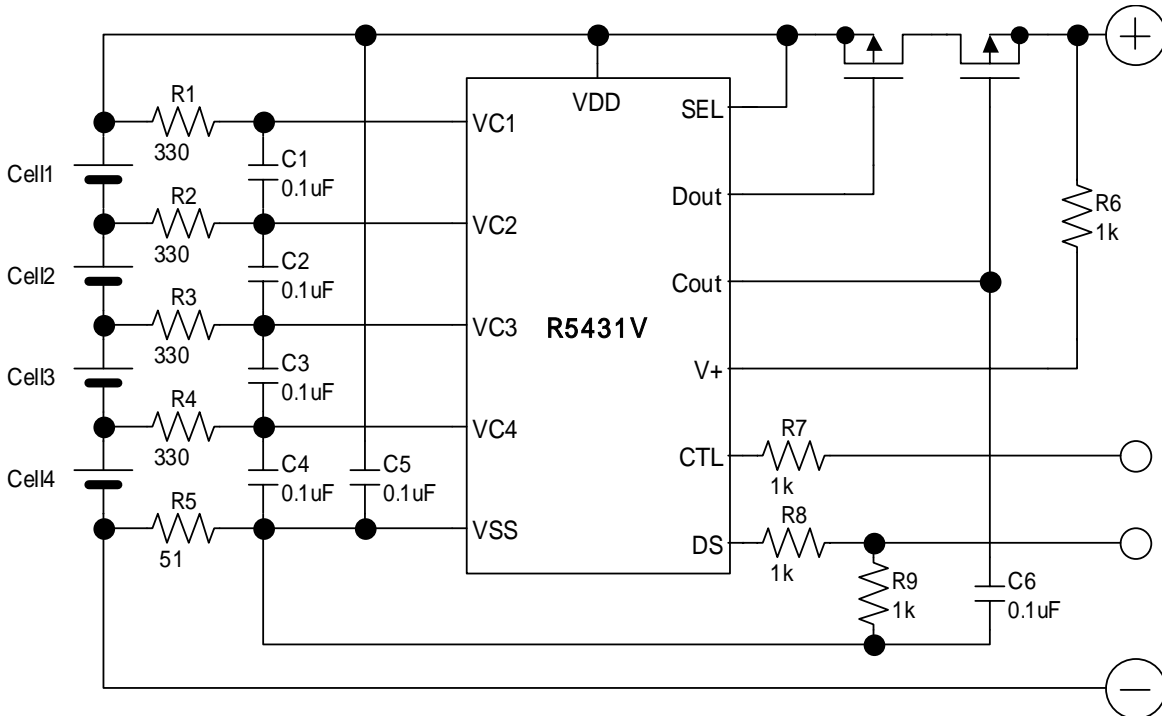


*Circuit example (for 3-cell protection with CTL function and DS function)
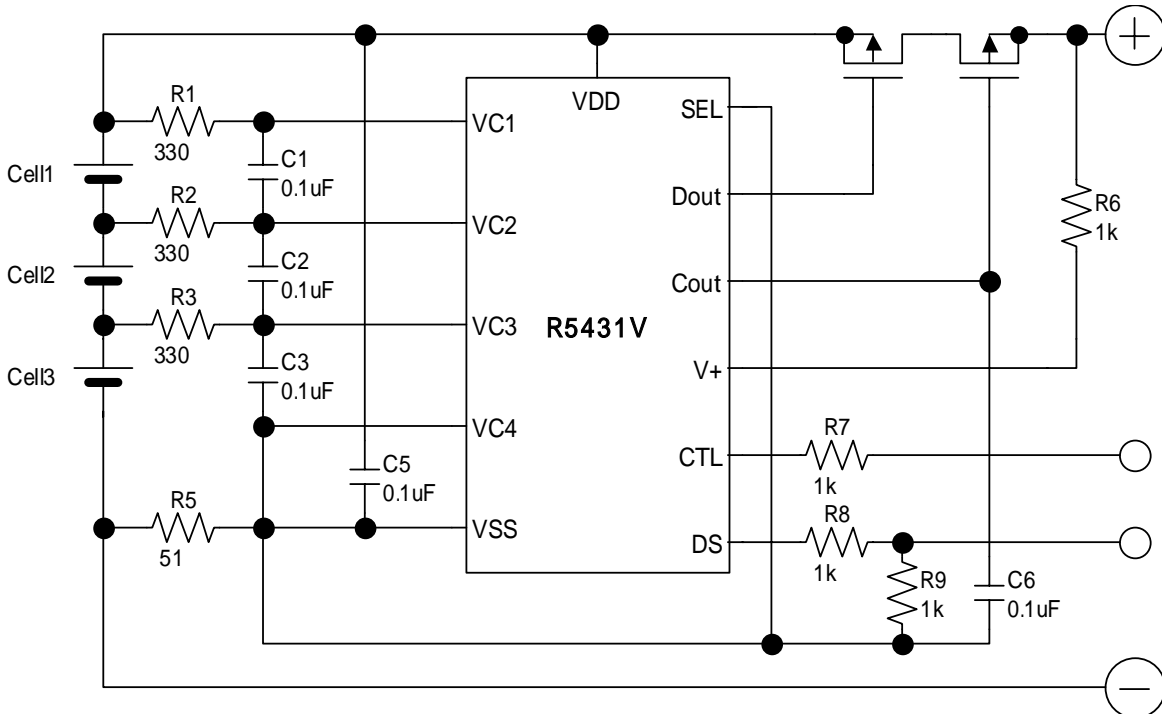
## TECHNICAL NOTES

R1, R2, R3, R4, R5, C1, C2, C3, C4, and C5 stabilize the supply voltage to the R5431Vxxxxx. If R1, R2, R3, R4, and R5 values are large, the conduction current inside the IC at detection mode, the detector threshold may rise, therefore recommended R1, R2, R3, R4 value is equal or less than 1kΩ. The recommended R5 value is equal or less than 330Ω.

To stabilize the operation, the value of C1, C2, C3, C4, and C5 should be equal or more than 0.01μF.

R5 and R6 can operate also as parts for current limit circuit against the reverse charge or applying a charger with excess charging voltage beyond the absolute maximum rating of the R5431Vxxxxx. Small value of R5 and R6 may cause over-power consumption rating of the power dissipation of the R5431Vxxxxx. Thus, the total value of 'R5+R6' should be equal or more than 1kΩ.

If R5 value is set too large, by the conduction current inside the IC at detection, the detector threshold becomes lower, thus recommended R5 value is equal or more than 330Ω. If R6 value is set too large, release operation by connecting a charger may be impossible, our recommendation value as R6 is equal or less than 10kΩ.

R7 and R8 can operate as parts for current limit circuit against forcing over voltage. If CTL function or CTL function is necessary, attach R7 and R8 with the resistance of 1kΩ or more. Since a pull-down resister is not built in the DS pin, when the DS function is necessary, attach R9 with the resistance of 1kΩ.

To stabilize the operation of the IC, use a capacitor with a range of the capacity from 0.06μF to 0.1μF as C6.

The typical application circuit diagram is just an example. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary. Over-voltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components. If positive terminal and negative terminal of the battery pack short, even though the short protection circuit is built in the IC, during the delay time until detecting the short-circuit, a large current may flow through the FET.

Select an FET with large enough current capacity in order to endure the large current during the delay time.

# TEST CIRCUITS

**A**

**E**

**B**

**F**

**C**

**G**

**D**

**H**

**I**



**M**



**J**



**N**



**K**



**L**
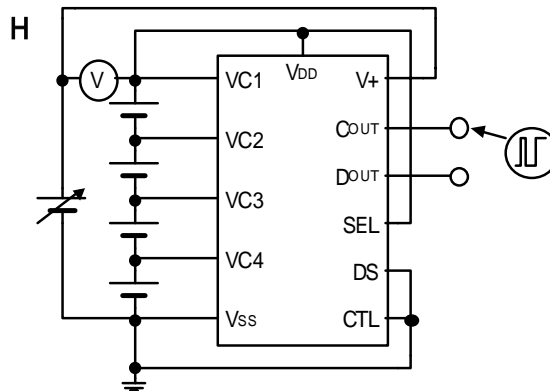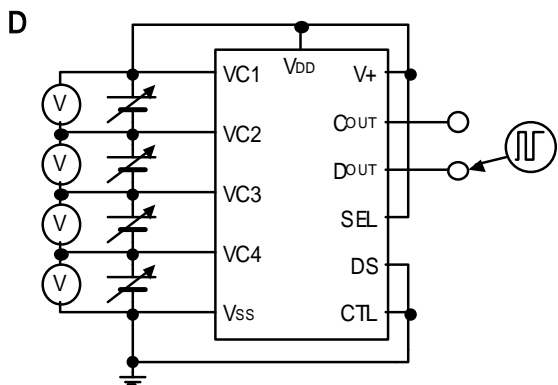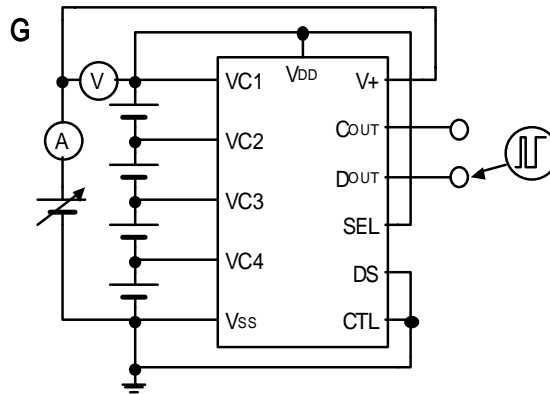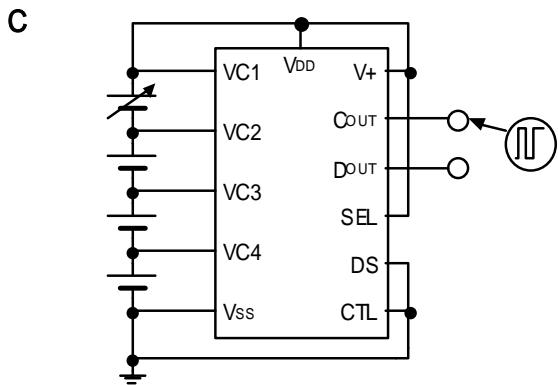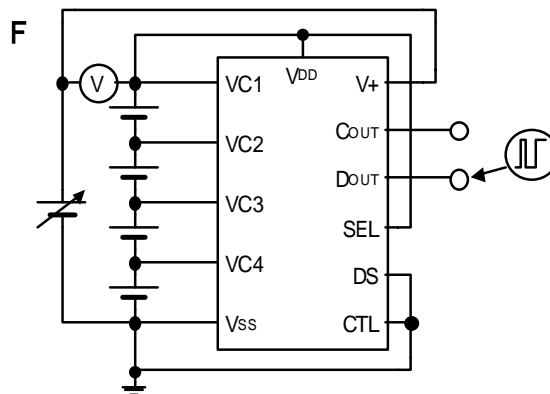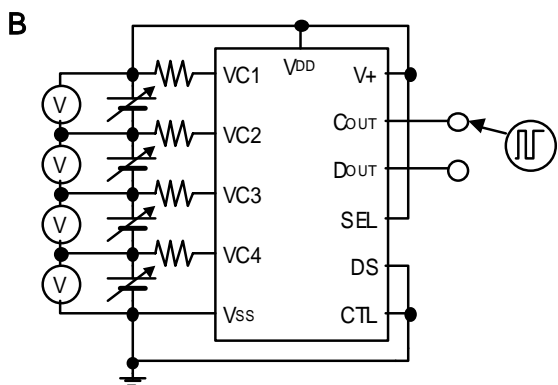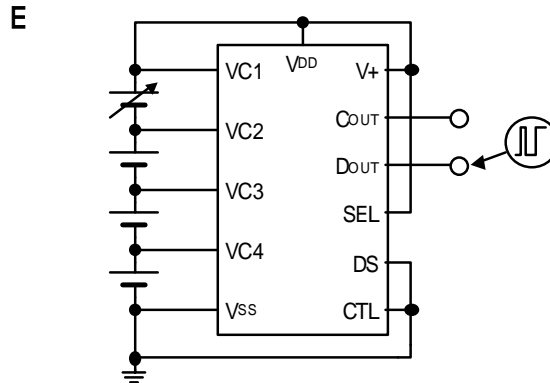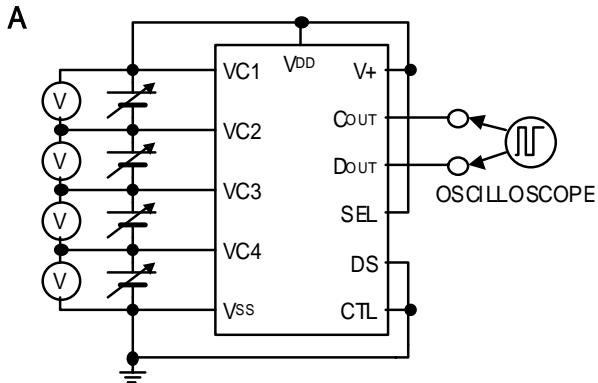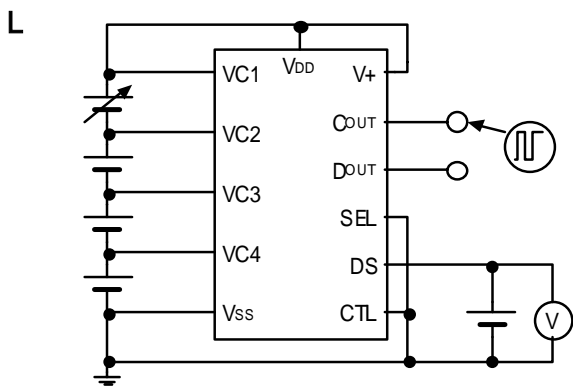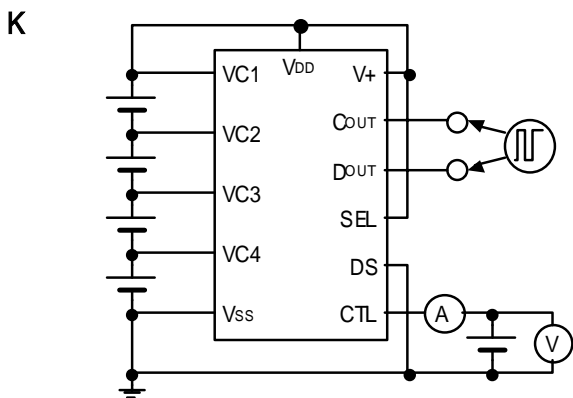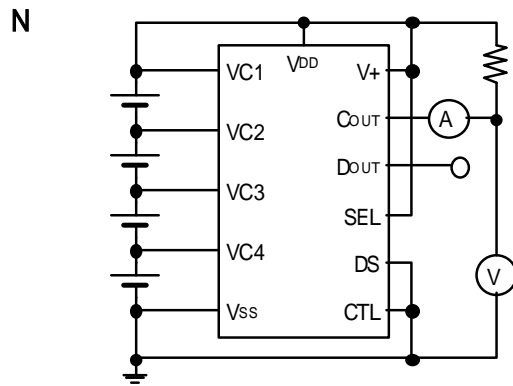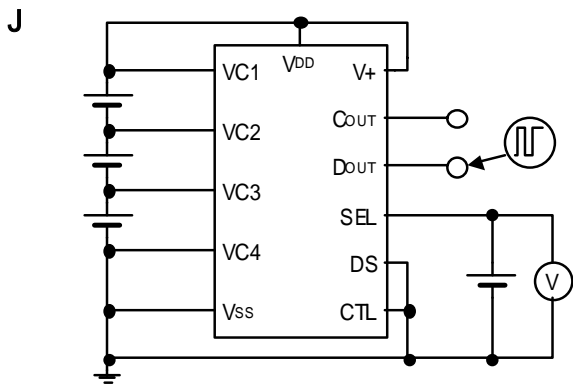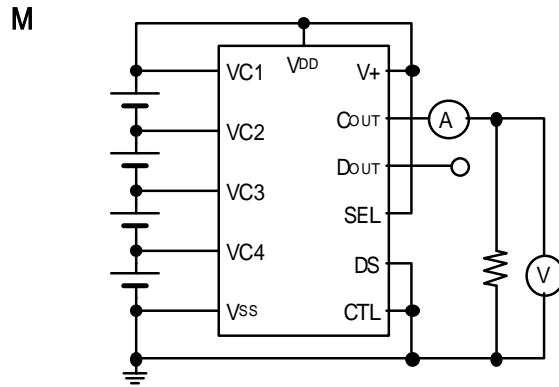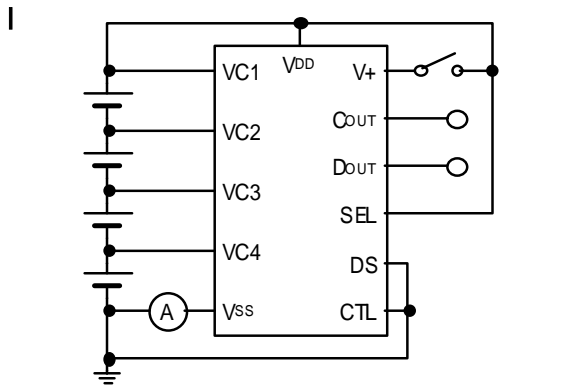
**Typical Characteristics were obtained with using those above circuits:**

Test Circuit A: Typical characteristics 1)
Test Circuit B: Typical characteristics 2) 3)
Test Circuit C: Typical characteristics 4) 5)
Test Circuit D: Typical characteristics 6) 7)
Test Circuit E: Typical characteristics 8) 9) 10)
Test Circuit F: Typical characteristics 11) 12) 13) 14) 15) 16) 17) 18) 19)
Test Circuit G: Typical characteristics 20)
Test Circuit H: Typical characteristics 21) 22) 23)
Test Circuit I: Typical characteristics 26)
Test Circuit J: Typical characteristics 24)
Test Circuit K: Typical characteristics 27)
Test Circuit L: Typical characteristics 25)
Test Circuit M: Typical characteristics 28)
Test Circuit N: Typical characteristics 29) 30)

# TYPICAL CHARACTERISTICS (Part 1)

1) Maximum charge inhibit voltage for CELLn vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=1.9V
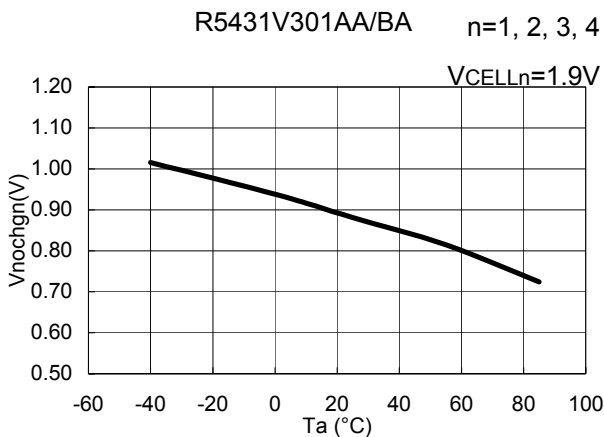
2) Over-charge voltage threshold (CELLn) vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4
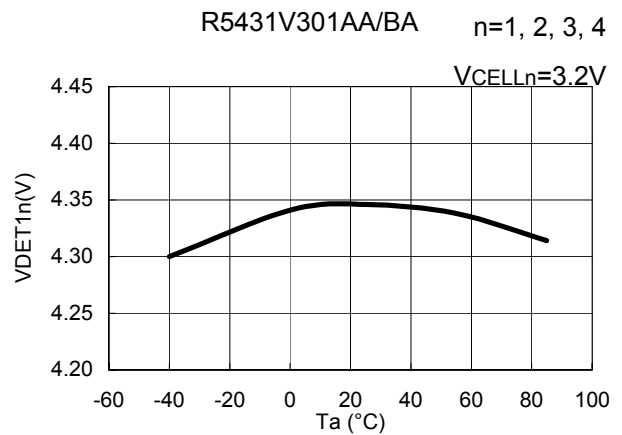
$V_{CELLn}$=3.2V

3) CELLn Over-Charge Released Voltage vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=3.2V

4) Over-charge Detector Delay Time vs. Temperature
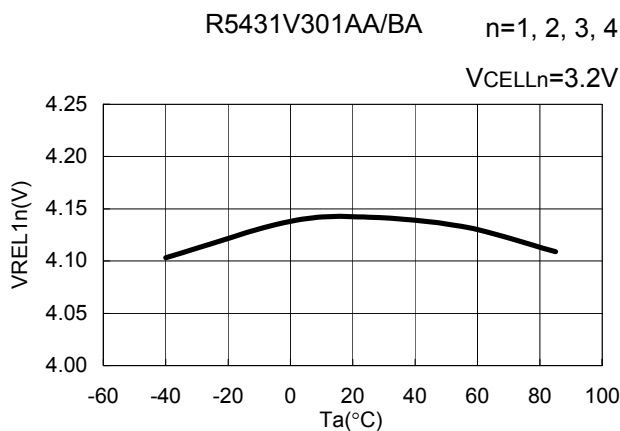
R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=3.5V, $V_{CELL1}$=3.5V to 4.5V
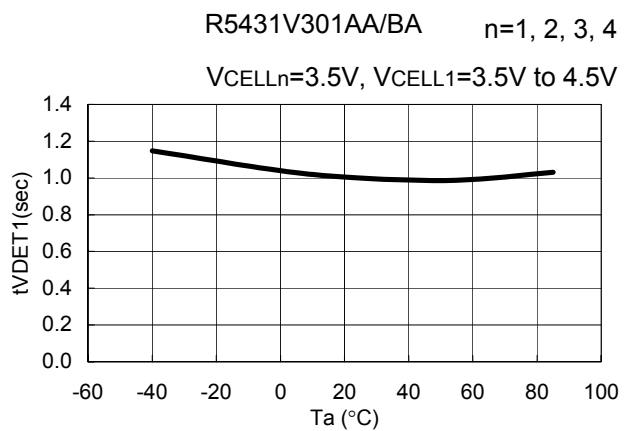
5) Release from Over-charge Delay Time vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

VCELLn=3.5V, VCELL1=4.5V to 3.5V
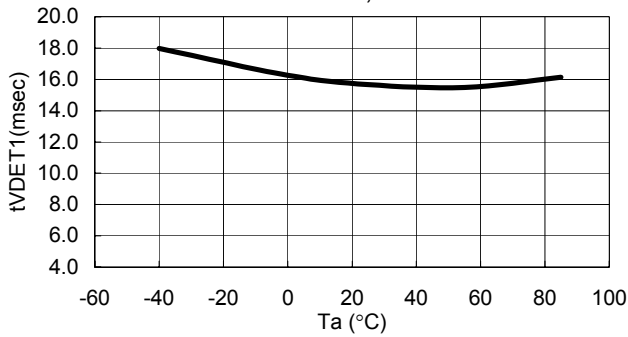


6) CELLn Over-discharge Detector Threshold vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4
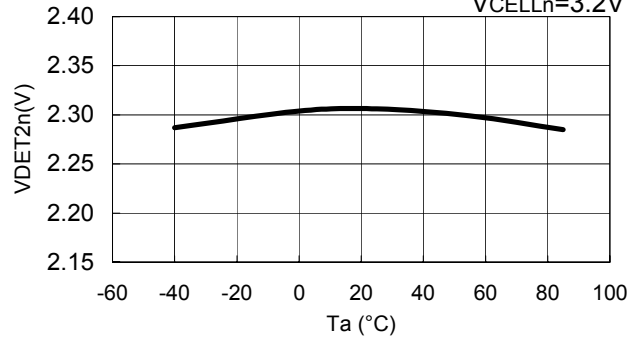
VCELLn=3.2V



7) CELLn Release Voltage from Over-discharge vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4
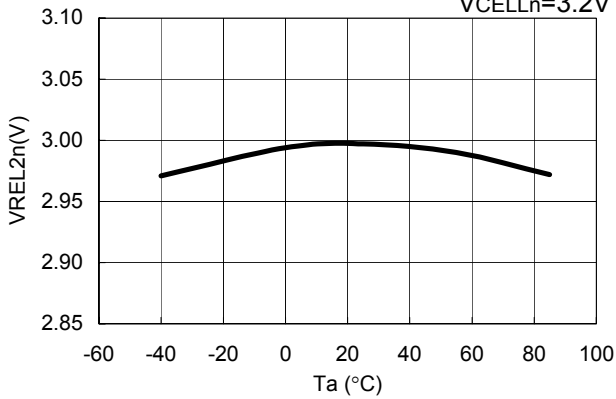
VCELLn=3.2V



8) Over-discharge Detector Delay Time vs. Temperature (Ver. AA)

R5431V301AA  n=1, 2, 3, 4

VCELLn=3.5V, VCELL1=3.5V to 2.0V
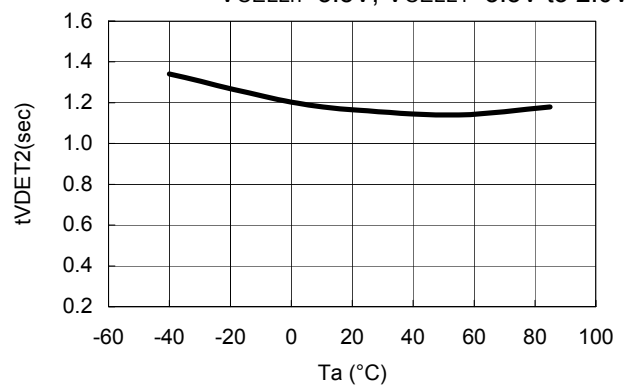


9) Output Delay Time of Over-discharge Detector vs. Temperature (Ver. BA)

R5431V301BA  n=1, 2, 3, 4

VCELLn=3.5V, VCELL1=3.5V to 2.0V
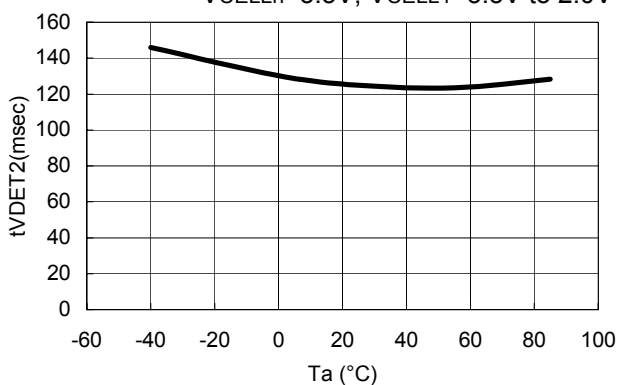


10) Output Delay Time of Release from Over-discharge vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

VCELLn=3.5V, VCELL1=2.0V to 3.5V
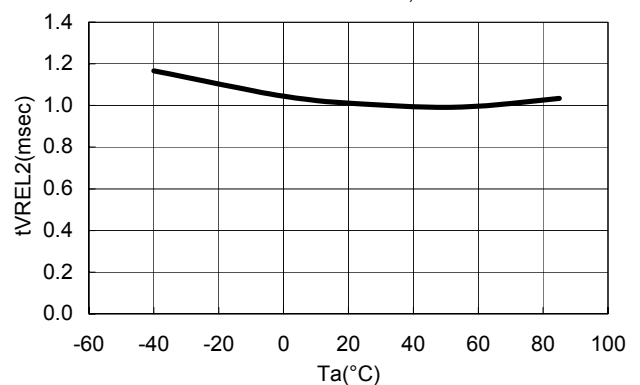
11) Excess Discharge Current Detector Threshold 1 vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

VCELLn=3.5V
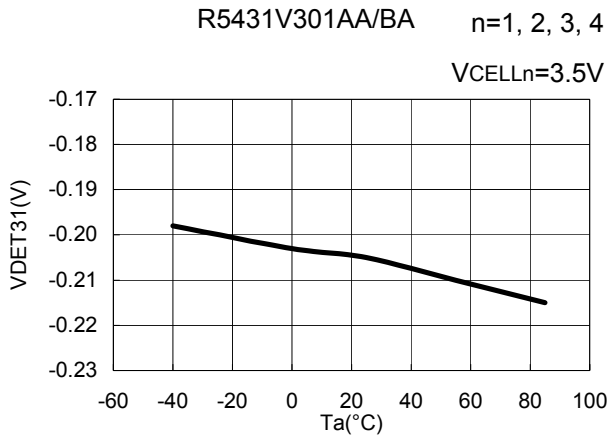


12) Excess Discharge Current Detector Threshold 2 vs. Temperature
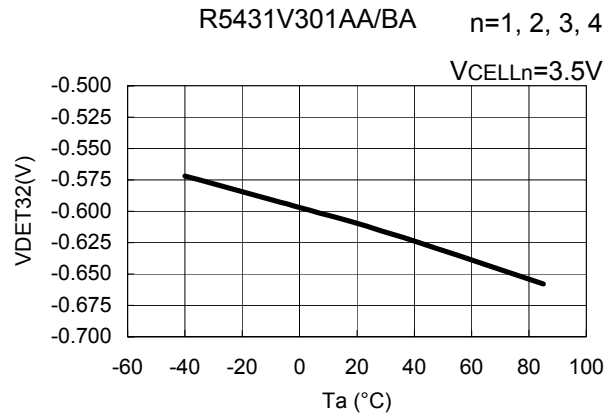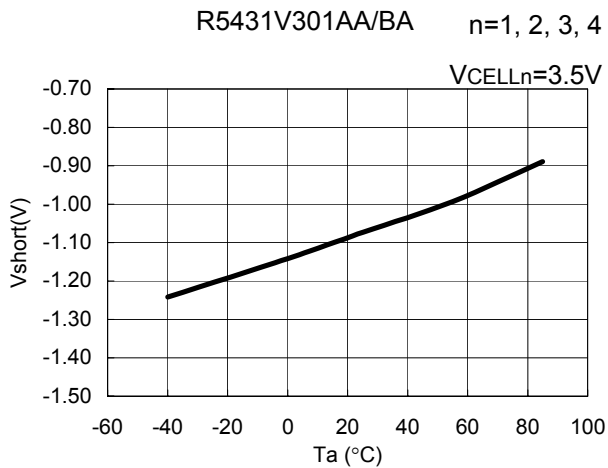
R5431V301AA/BA  n=1, 2, 3, 4

VCELLn=3.5V



13) Short Detector Threshold vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

VCELLn=3.5V



14) Output Delay Time of Excess discharge Current Detector 1 vs. Temperature (Ver. AA)

R5431V301AA  n=1, 2, 3, 4

VCELLn=3.5V, V+=14.0V to 13.6V



15) Output Delay Time of Excess discharge-current Detector 1 vs. Temperature (Ver. BA)

R5431V301BA  n=1, 2, 3, 4

VCELLn=3.5V, V+=14.0V to 13.6V



16) Output Delay Time of Excess Discharge Current Detector 2 vs. Temperature (Ver. AA)

R5431V301AA  n=1, 2, 3, 4

VCELLn=3.5V  V+=14.0V to 13.3V

17) Output Delay Time of Excess Discharge Current Detector 2 vs. Temperature (Ver. BA)

R5431V301BA  n=1, 2, 3, 4

$V_{CELLn}$=3.5V, V+=14.0V to 13.3V
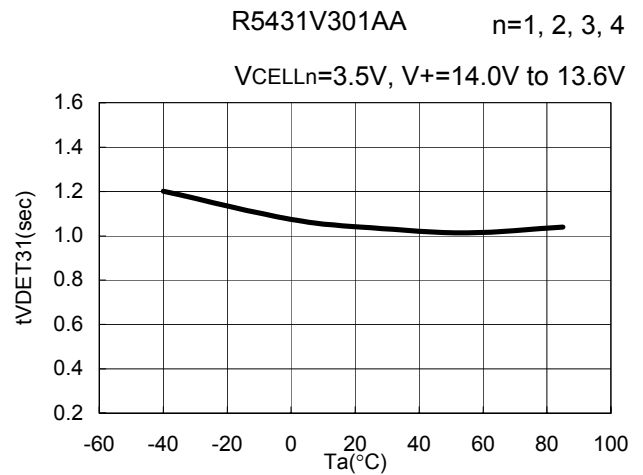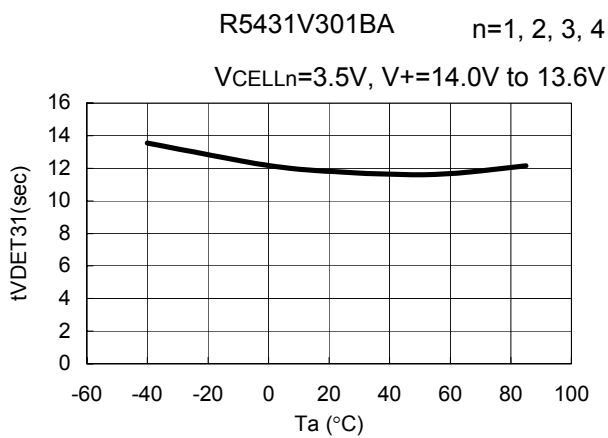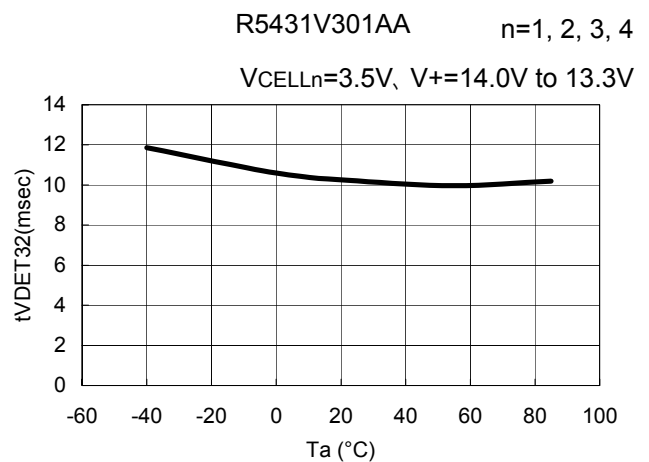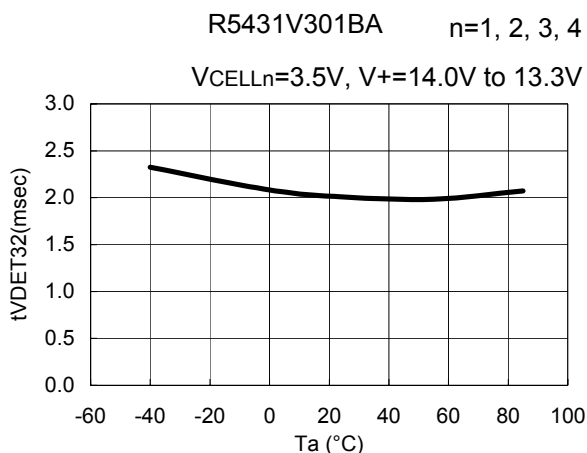


18) Output Delay Time of Short Detector vs. Temperature vs. Temperature
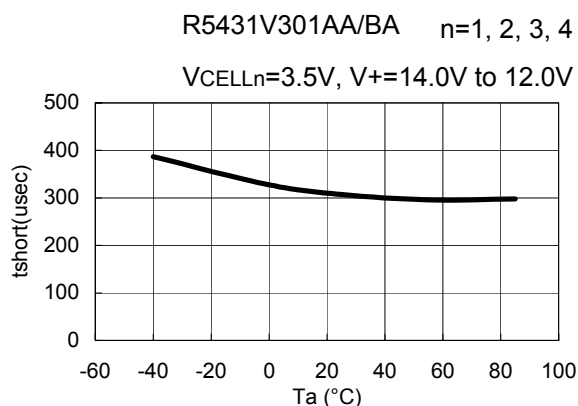
R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=3.5V, V+=14.0V to 12.0V



19) Output Delay Time for Release from Excess-discharge current. vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=3.5V, V+=12.0V to 14.0V
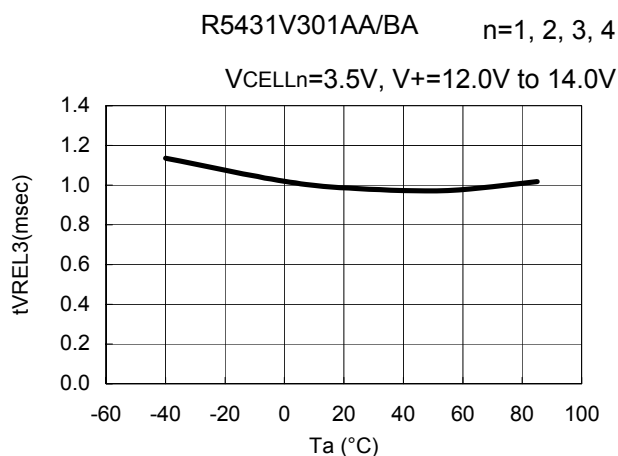


20) Excess Discharge Current Release Resistance vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

V+=$V_{DD}$-1.0V



21) Excess Charge Current Detector Threshold vs. Temperature

R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=3.5V
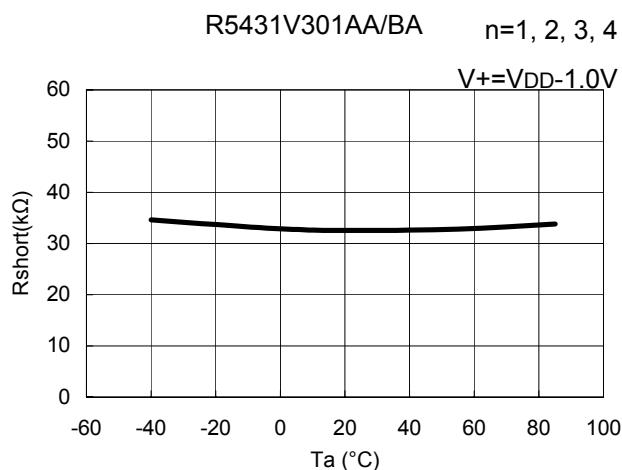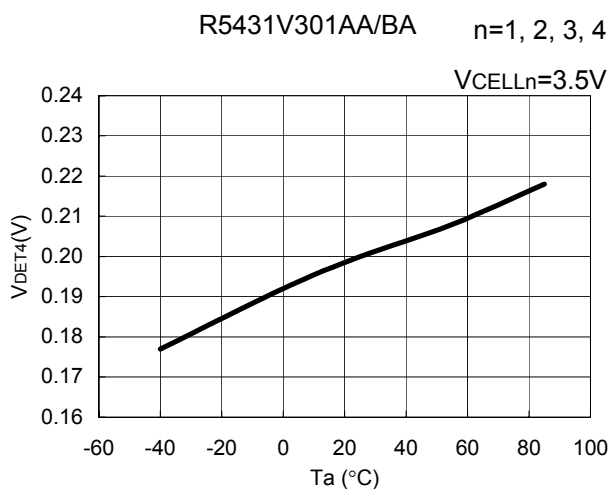


22) Output Delay Time of Excess Charge Current Detector vs. Temperature
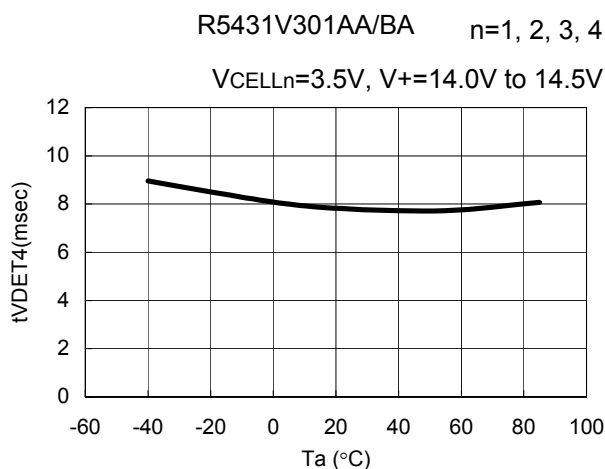
R5431V301AA/BA  n=1, 2, 3, 4

$V_{CELLn}$=3.5V, V+=14.0V to 14.5V

23) Output Delay Time of Release from Excess charge current vs. Temperature

R5431V301AA/BA    n=1, 2, 3, 4

VCELLn=3.5V, V+=14.5V to 14.0V



24) C$_{OUT}$ Nch ON Voltage vs. Temperature

R5431V301AA/BA    n=1, 2, 3, 4

IOL=-50uA



25) D$_{OUT}$ Nch ON Voltage vs. Temperature

R5431V301AA/BA    n=1, 2, 3, 4

IOL=-50uA



26) C$_{OUT}$ Pch ON Voltage vs. Temperature

R5431V301AA/BA    n=1, 2, 3, 4

IOH=50uA



27) D$_{OUT}$ Pch ON Voltage vs. Temperature

R5431V301AA/BA    n=1, 2, 3, 4

IOH=50uA
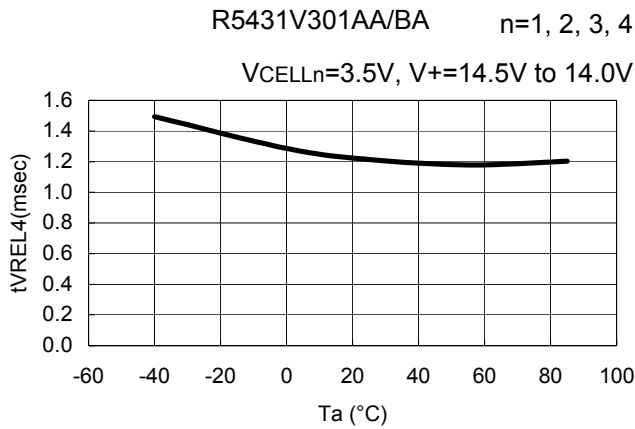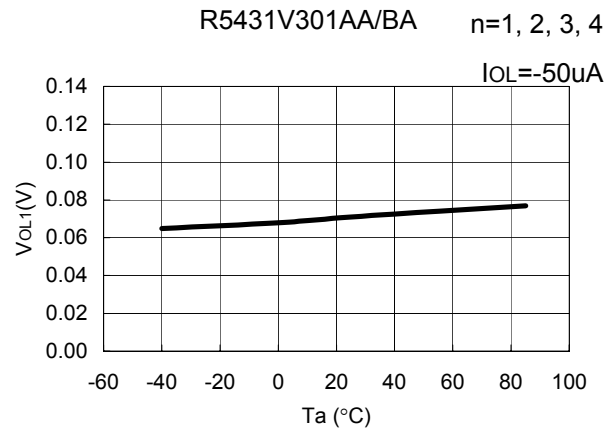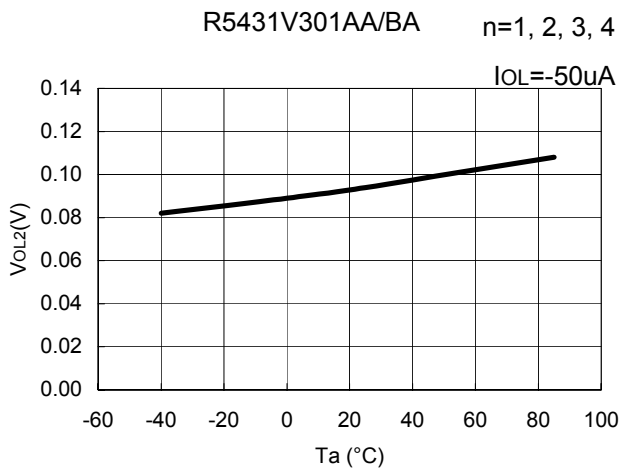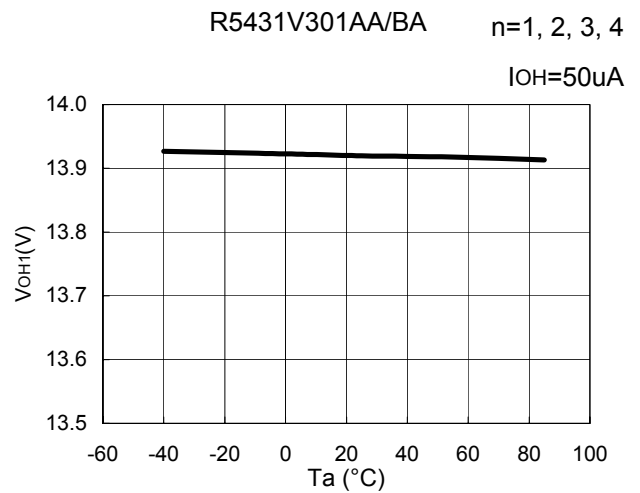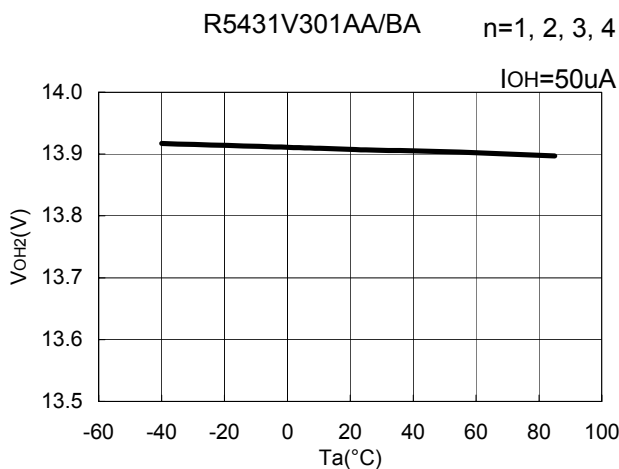


28) CTL pin "H" Input Current vs. Temperature

R5431V301AA/BA    n=1, 2, 3, 4

VCELLn=3.5V, CTL=VDD
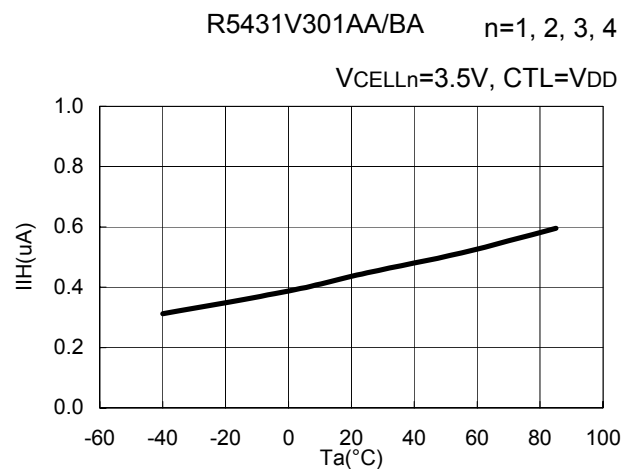
29) Supply Current (4-cell protection) vs. Temperature

R5431V301AA/BA     n=1, 2, 3, 4

VCELLn=3.9V
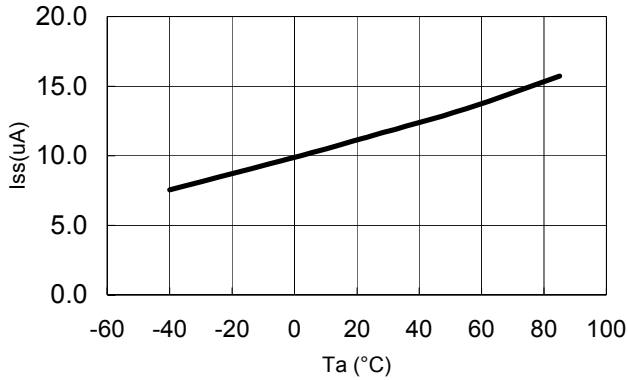


30) Standby Current (4-cell protection) vs. Temperature

R5431V301AA/BA     n=1, 2, 3, 4

VCELLn=2.0V
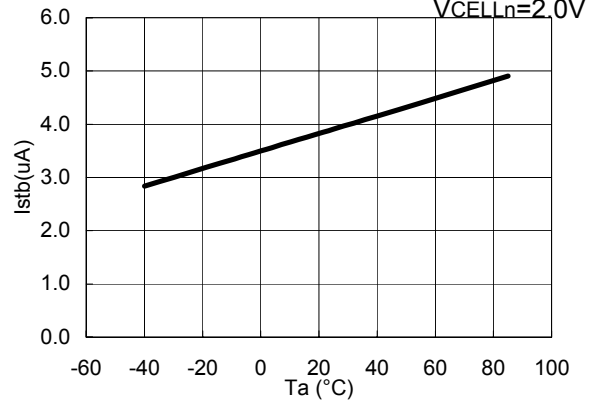


## Part 2. Delay Time dependence on $V_{DD}$

1) Delay Time for Over-charge detector vs. $V_{DD}$

R5431V301AA/BA
VCELL1=3.2V, 3.6V, 4.0V to 4.5V, SEL=VDD



n=1, 2, 3, 4
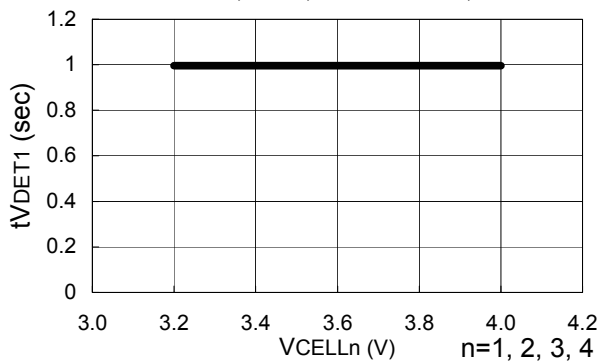
2) Delay Time for Release from Over-charge vs. $V_{DD}$

R5431V301AA/BA
VCELL1=3.2V, 3.6V, 4.0V to 4.5V, SEL=VDD



n=1, 2, 3, 4
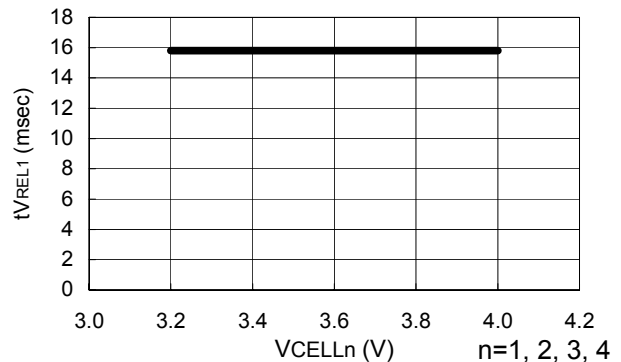
3) Output Delay of Over-discharge Detector vs. $V_{DD}$

(Ver. AA)

R5431V301AA
VCELL1=3.2V, 3.6V, 4.0V to 2.0V, SEL=VDD



n=1, 2, 3, 4
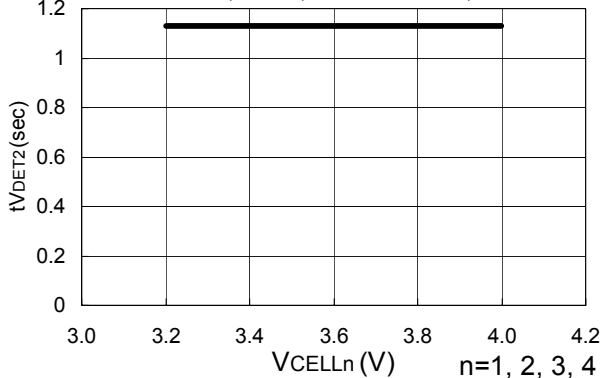
4) Output Delay of Over-discharge Detector vs. $V_{DD}$

(Ver. BA)

R5431V301BA
VCELL1=3.2V, 3.6V, 4.0V to 2.0V, SEL=VDD



n=1, 2, 3, 4

5) Output Delay of Release from Excess Discharge Current vs. $V_{DD}$
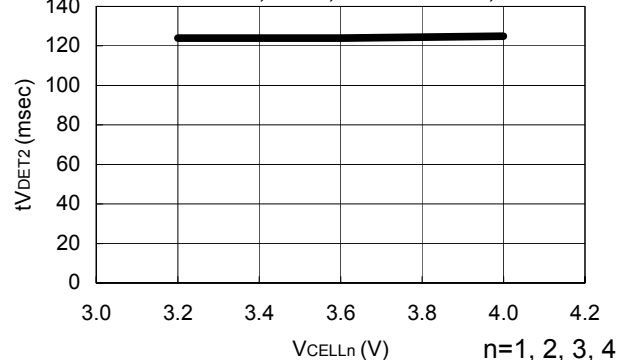
R5431V301AA/BA
VCELL1=3.2V, 3.6V, 4.0V to 2.0V, SEL=VDD



6) Output Delay of Excess Discharge Current 1 vs. $V_{DD}$
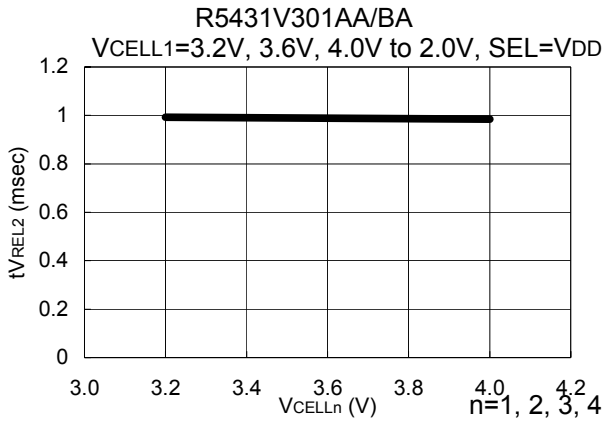
R5431V301AA
V+=VDD toVDD-0.3V, SEL=VDD
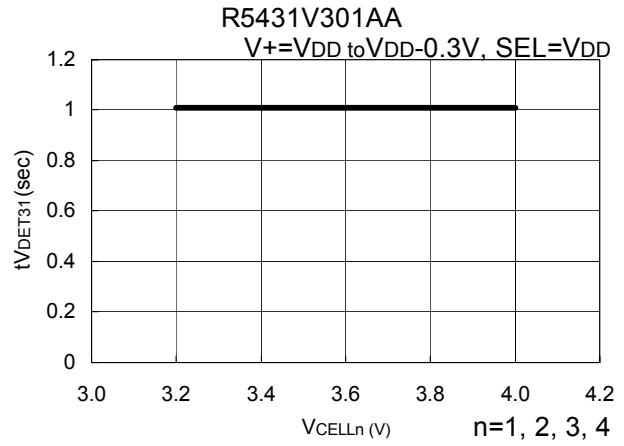


7) Delay Time of Excess Discharge Current Detector 1 vs. $V_{DD}$ (Ver,. BA)
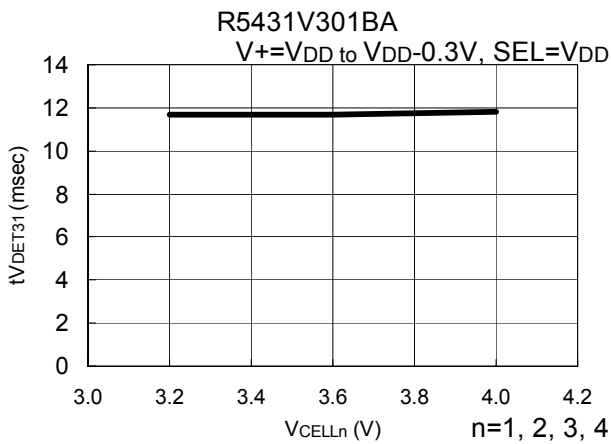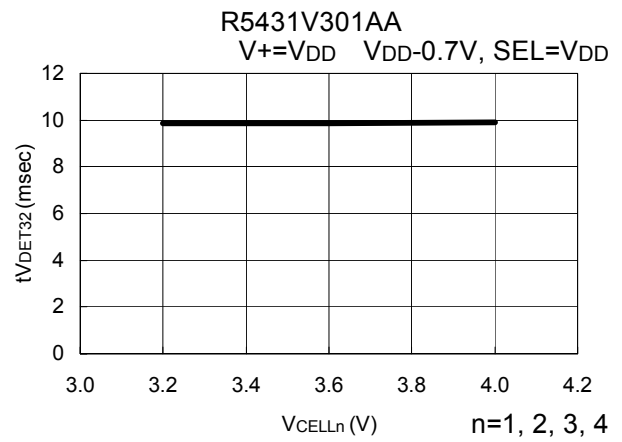
R5431V301BA
V+=VDD to VDD-0.3V, SEL=VDD



8) Delay Time of Excess Discharge Current Detector 2 vs. $V_{DD}$ (Ver. AA)

R5431V301AA
V+=VDD    VDD-0.7V, SEL=VDD



9) Delay Time of Excess Discharge Current Detector 2 vs. $V_{DD}$ (Ver. BA)

R5431V301BA
V+=VDD to VDD-0.7V, SEL=VDD



10) Delay Time of Short Detector vs. $V_{DD}$

R5431V301AA/BA
V+=VDD to VDD-2.0V, SEL=VDD
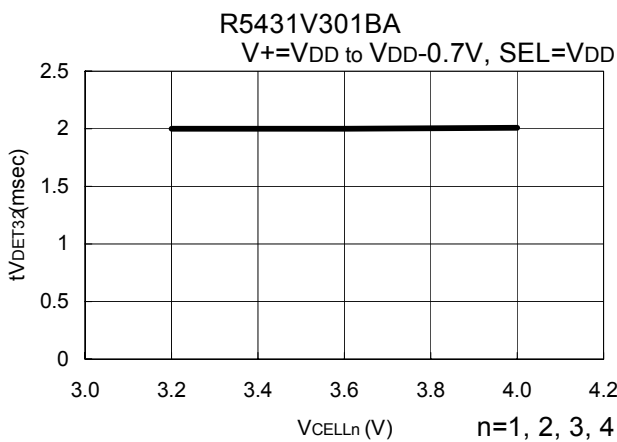
11) Delay Time of Release from Excess discharge current vs. VDD
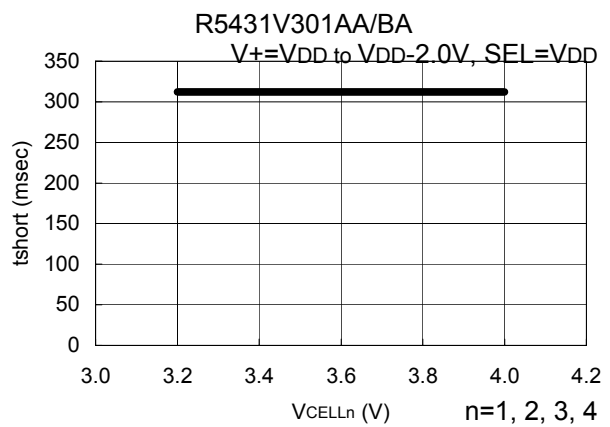
R5431V301AA/BA
V+=VDD-2.0V to VDD, SEL=VDD



12) Delay Time of Excess Charge Current Detector vs. VDD

R5431V301AA/BA
V+=VDD to VDD+0.5V, SEL=VDD
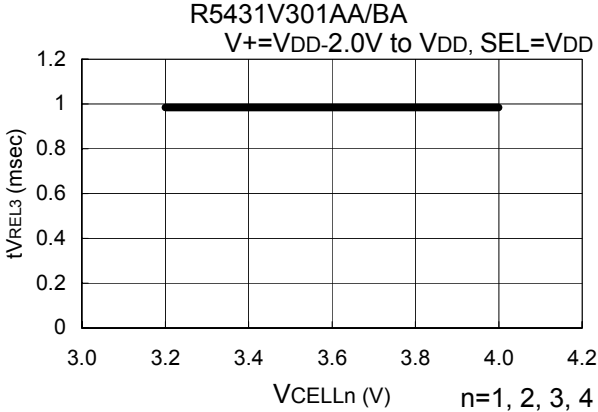


13) Delay Time of Release from Excess Charge Current vs. VDD
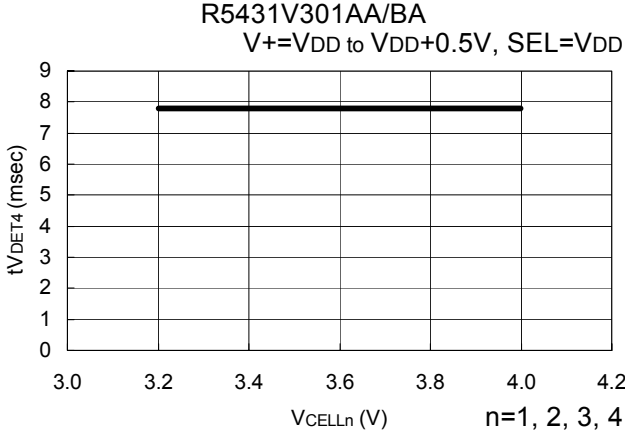
R5431V301AA/BA
V+=VDD    VDD+0.5V, SEL=VDD
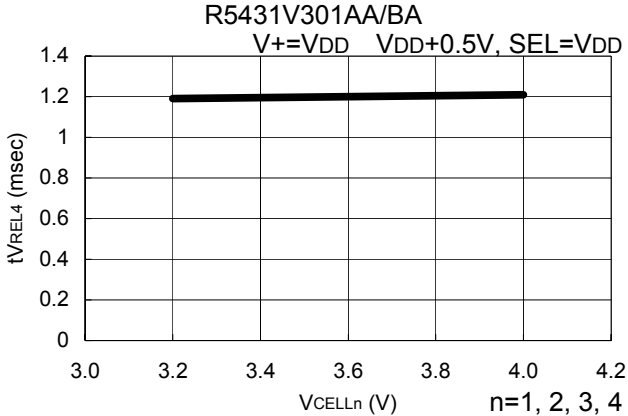
## Part 3   Supply Current dependence on V<sub>DD</sub>

**Test Circuit (for 4-cell protection)**
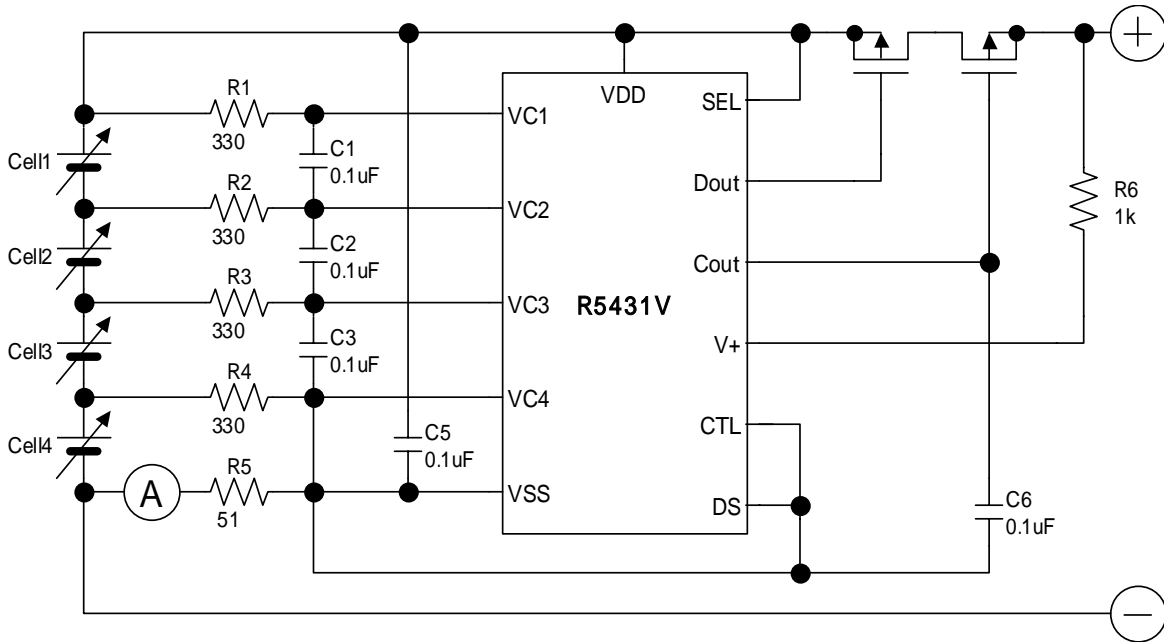


**4-cell protection Supply Current vs. V<sub>DD</sub>**
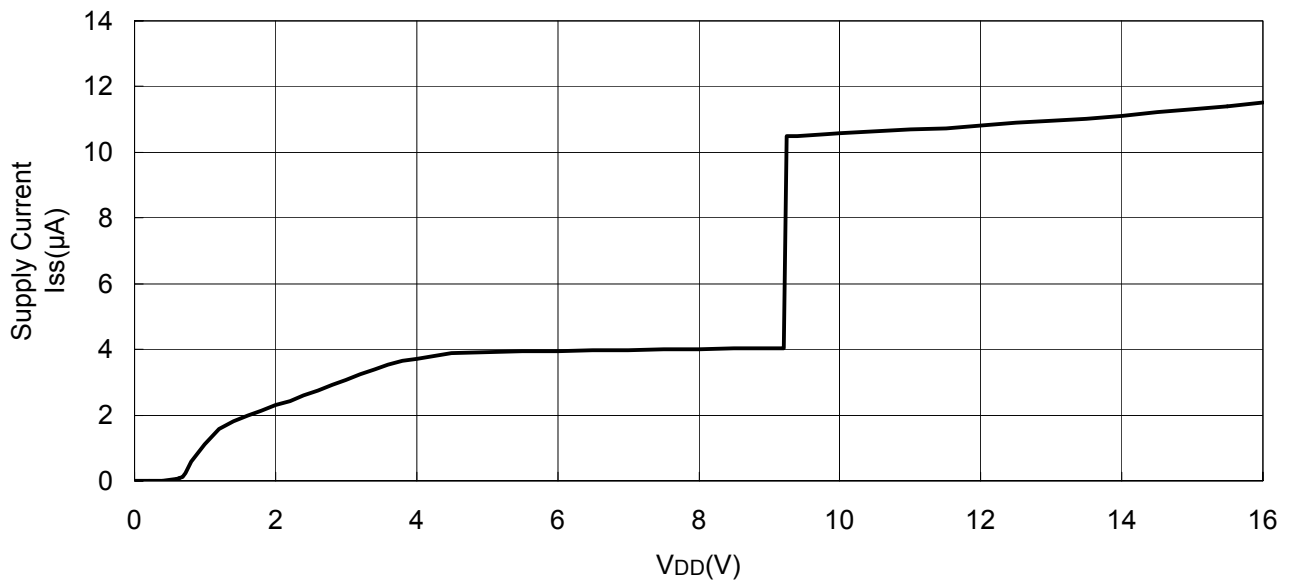
**Part 4    Over-charge detector, Release voltage from Over-charge, Over-discharge detector, Release voltage from Over-discharge dependence on External Resistance value**
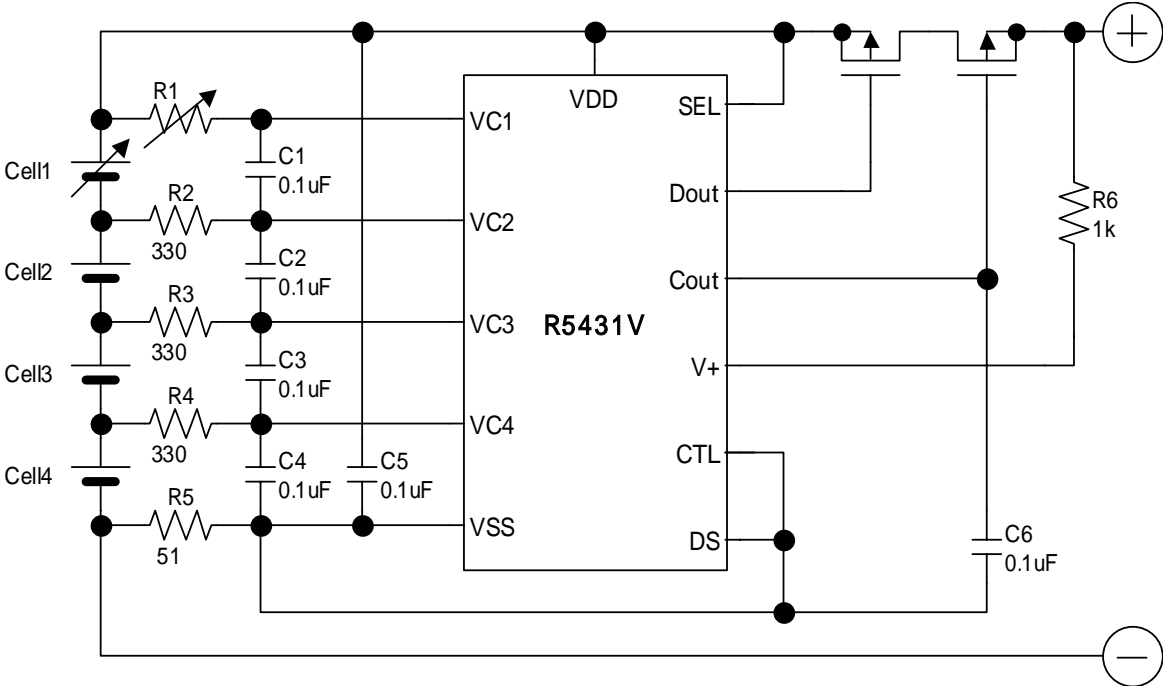


**Test Circuit**

Over-charge Detector Threshold / Released Voltage from Over-charge vs. R1 (CELL1)
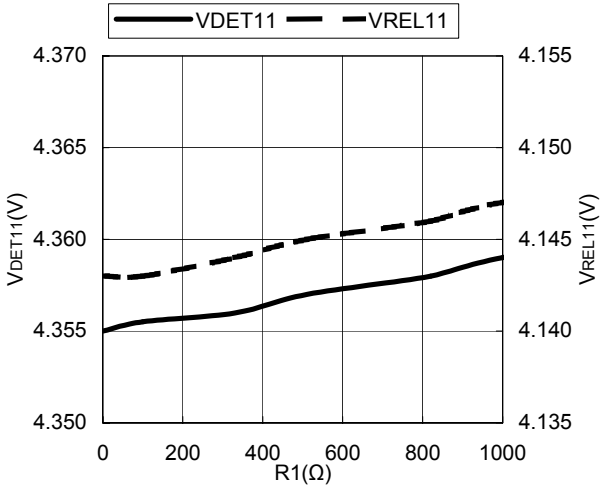


Over-discharge / Released from Over-discharge Threshold vs. R1 (CELL1)

# RICOH COMPANY., LTD.  Electronic Devices Company

■**Ricoh presented with the Japan Management Quality Award for 1999.**
Ricoh continually strives to promote customer satisfaction, and shares the achievements of its management quality improvement program with people and society.

日本経営品質賞
1999年度受賞

■**Ricoh awarded ISO 14001 certification.**
The Ricoh Group was awarded ISO 14001 certification, which is an international standard for environmental management systems, at both its domestic and overseas production facilities. Our current aim is to obtain ISO 14001 certification for all of our business offices.

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RoHS Compliant

Ricoh completed the organization of the Lead-free production for all of our products. After Apr. 1, 2006, we will ship out the lead free products only. Thus, all products that will be shipped from now on comply with RoHS Directive.