THIS IS NOT INTENDED AS A PROJECT AND WILL NOT BE SUPPORTED AS SUCH. DO NOT CALL US.

Service manual for D-1 DAC

The D-1 Dac contains 3 separate printed circuit boards in it's chassis. They are the motherboard, receiver board and front panel display and control board.

The motherboard has test points for all the on board power supply voltages. These points are located by the heat sinks and labeled on the silk screen. The plus and minus 20 digital are unregulated and are approximate voltages. There are separate 5-volt regulators on the motherboard for VCO and PLL circuits. The receiver board and front panel boards have their own 5-volt regulators.

The receiver-input selection is controlled by the front panel microprocessor via Mosfets. These switch one of four relays on the receiver board. The signal is routed to a Crystal 8412 receiver chip. The output of the Crystal chip is feed to the NPC digital filter and also to U7 PLL on the motherboard for the PLL reference. The master clock from the 8412 is feed to the front panel board and used to determine sampling frequency. The sampling frequency determines the selection of signals F0 and F1 for proper VCO crystal selection and digital filter deemphasis selection. F0 and F1 come from the microprocessor on the front panel to the motherboard and the receiver board via a ribbon cable. The front panel also sends the polarity signal to the receiver board.

U7 and U4 along with VCO module U3 form a secondary PLL circuit to clock the digital filter and DAC's. U5 and U2 are separate regulators for the VCO and PLL chips. R5 and R6 along with C13 form the PLL filter. When the system is locked U7 pins 3 and 14 are at the word clock rate (44.1 for cd).

The receiver boards digital filter feeds buffers U9 and U10 on the mother. These signals are then routed to the PCM 63's via resistors. The left and right channels are identical.

The analog section consists of four matched Mosfets for each channel. Two for current to voltage conversion and two for output buffers. The current to voltage converter transistors Q3 and Q6 have their sources adjusted to 0 volts + or – 50 mV with trim pots.

The drains run at about 17 volts. The output buffers Q2 and Q5 have their drains at the supply rails of 33 volts. The sources run at about 14 volts. The volume control works by coupling the drains of the current to voltage converter transistors through fixed resistors and a switch. This sums opposite phases and cancels some of the signal. The analog signal is then routed to the buffers gates and out it's sources to the output jacks. The signal is muted with two relays in case of a power failure or when the Crystal receiver has lost lock.

Revision notes

REV1: PC board physical layout changes for better parts fit.
Silk screen now lists component values instead of reference designators.
Mute circuit has delay added on U3 receiver board.

FIRST RUN SHIPPED

Title	PL55 MOTHER BOARD		
Size D	Number		Rev R0
Date 12-11-97	Drawn by WAYNE COLBURN		
Filename PL55MTHR0.SCH	Sheet 1 of 4		

TO DAUGHTER BOARD

IDC2X10M — P1:2 — P1:1 — +15VD

TO DAUGHTER BOARD

IDC2X10M — P3:2 — FS 44.1KHZ — SN74HC02N — JUMPER FOR 96K — JUMPER FOR 44.1K — U4

512 FS 22.5792 MHZ — U3

U7 — 74HC4046 — 44.1

+15VD — LM78L05ACZA — U5 — C4 220UF/16V — C8 .1 — C14 220UF/16V — C9 .1 — R4 22 — R7 2.2M — R6 15K — R5 3.32K — C13 4.7UF — C12 .01PP

+15VD — LM78L05ACZA — U2 — C5 220uf — C3 .1 — C11 220uf — C6 .1 — R3 22

TO PL55 FRONT PANEL PCB

IDC2X10M — P2:1 — +15VD — POLARITY — LOCKL — FI — FO — IN1 — IN2 — IN3 — IN4 — P2:2 — 256/OUT

MUTE RELAYS

K1 — K2 — +MUTE — -MUTE — 9610 — R39 4.75K — +42 — +30 — Q7 — R36 22.1K — D15 1N4007 — D6 1N4739 — C61 220UF — D1 1N4739 — Q8 610 — Q4 IRF610 — R2 100K — LOCKL — R1 10K — Q1 ZTX550 — +5VD

+15VD — U19 7815 — R40 1.5K — C74 220UF50V — D4 1N4739 — D2 1N4739 — D3 1N4739 — D5 1N4739 — R18 1.5K — U20 7915 — -30 — C75 220UF50V — C93 10000UF — C92 10000UF — D7 — D8 — D9 — D10 — PAD104 — PAD105 — PAD106 — +42

+15VD — U8 7815 — C7 .1 — C10 220UF/16V — C18 — 20VD — C26 3300UF35V — C37 3300UF35V — C38 3300UF35V — C27 3300UF35V — D11 — D12 — D13 — D14 — PAD100 — PAD102 — PAD103 — C2 .1 — C1 220UF16V — C19 .1 — U11 7915 — -15VD

GNDDIGITAL — PAD101

LEFT CHANNEL SHOWN

GNDANALOG — C51 .15 — C50 220UF/16V — C57 .15 — C56 220UF/16V — C48 .15 — C47 220uf — U17 PCM63 — SN74HC86N — U9:B — R8 150 — R10 150 — R13 150 — VDD — GNDDIGITAL — C67 .15 — C66 220UF/16V — C54 .15 — C53 .15 — C52 .15 — C49 220UF/16V — C62 .15 — C60 220UF/16V — -5VD — +5VD — +5V — -5V

LEFT CHANNEL SHOWN

-OUT — C59 .047 — R30 22K — -MUTE — R29 150 — C58 220UF/16V — PAD109 — GNDANALOG — .0047PF — C43 — C21 220UF/16V — R23 22K — +OUT — PAD108 — PAD107 — +MUTE — R22 150 — C20 .047 — +OUT

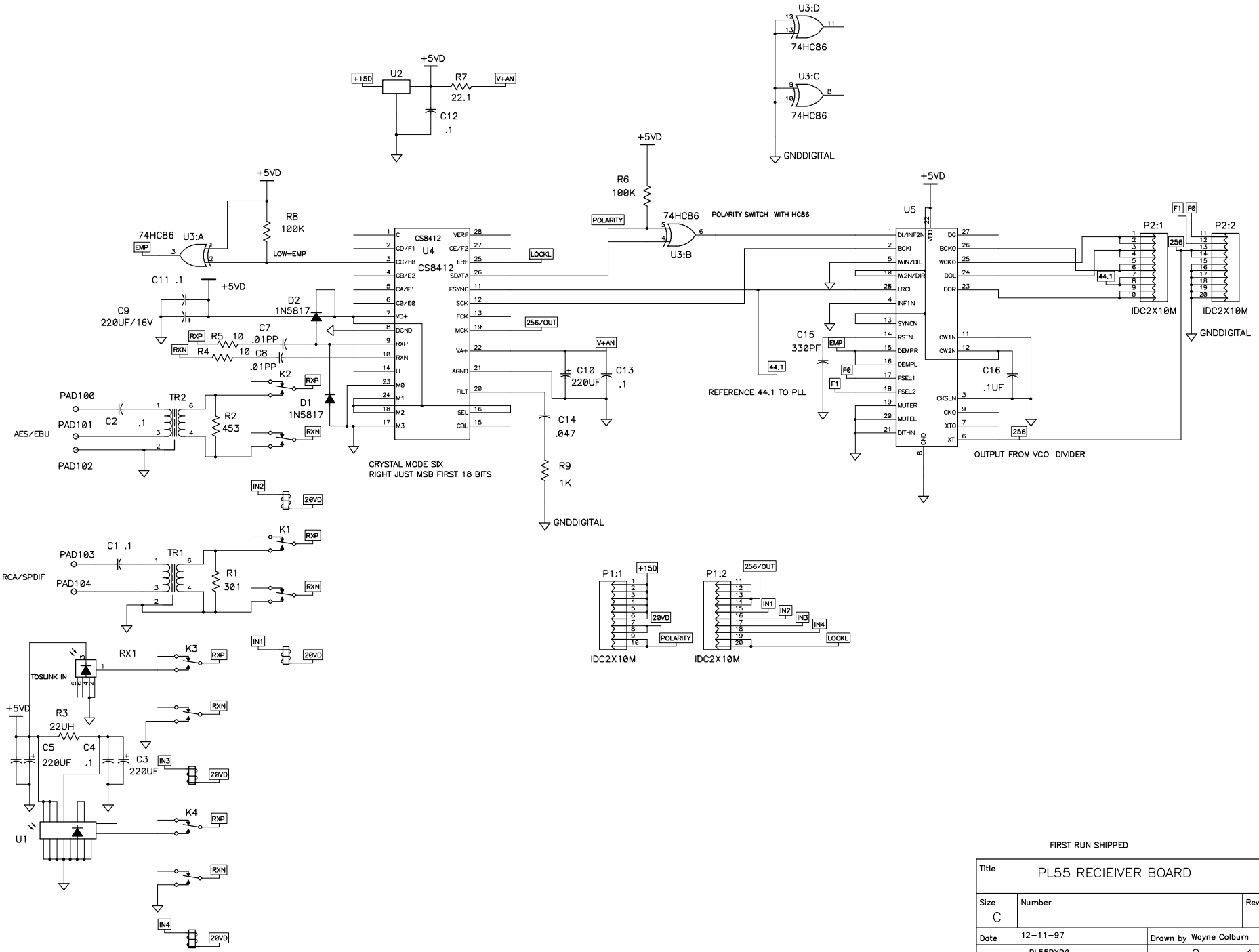
LEFT CHANNEL SHOWN

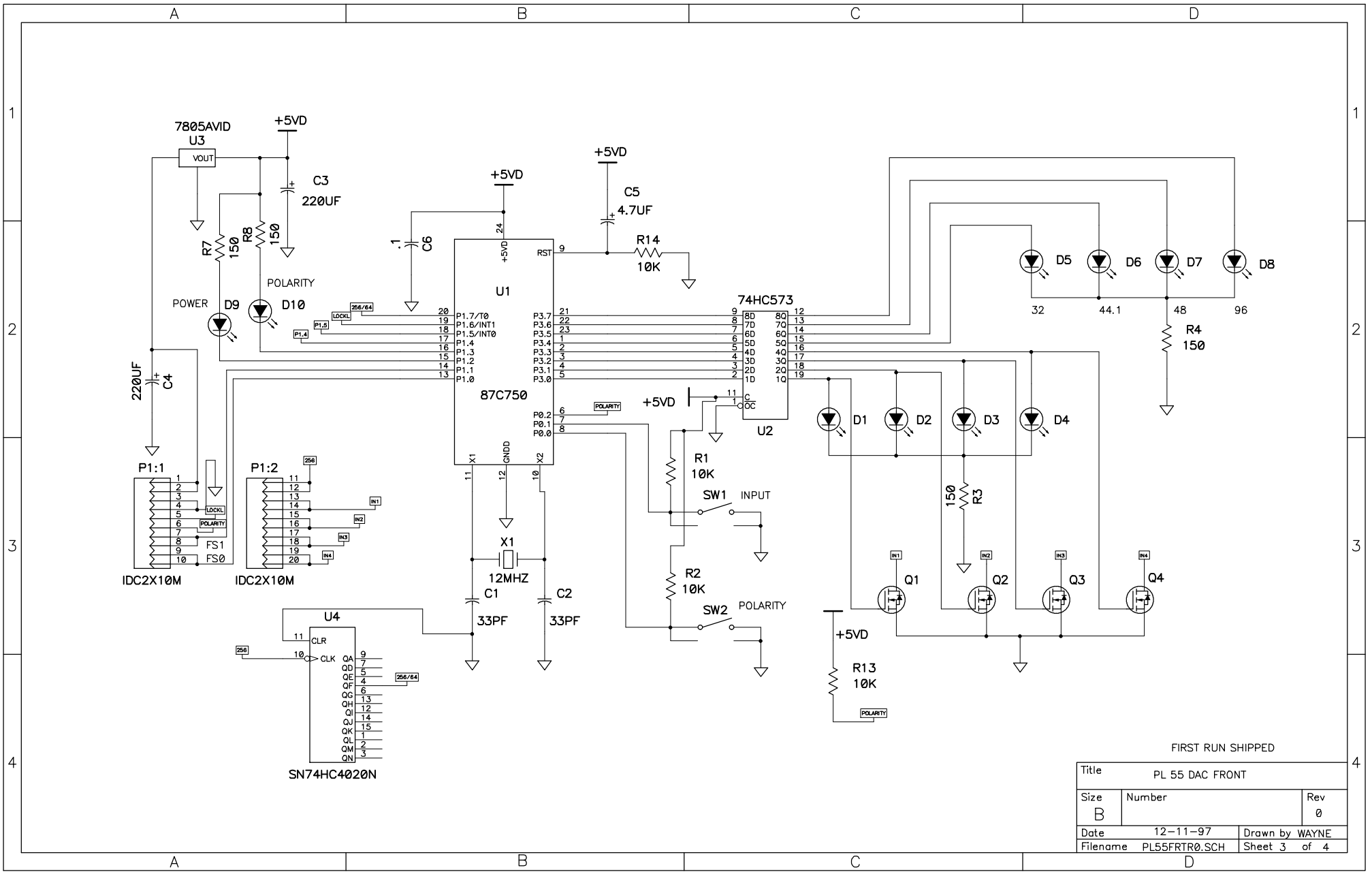
C23 220UF/16V — C33 220uf — C34 .15 — C24 .15 — C29 .15 — C28 220UF/16V — U12 PCM63 — SN74HC86N — U9:A — SN74HC86N — U9:D — SN74HC86N — U9:C — R9 150 — R11 150 — R12 150 — DOR — P3:1 — 44.1 — TO DAUGHTER BOARD — IDC2X10M

-30 — C45 220UF/50V — R28 10 — C40 .01 — R26 3.3K — R33 3.3K — C55 .01 — R35 221 — P5 20K — Q6 610 — Q3 610 — P4 20K — R21 221 — C22 220UF/16V — C65 220UF/16V — VOL- — VOL+ — C44 220UF/50V — R32 1.5K — R34 1.5K — R25 1.5K — R27 1.5K — Q5 610 — Q2 610 — R31 100K — R24 100K — C15 .0027UF — C16 .0027UF — R20 10 — +30 — -5VD — +5VD — +5V — -5V — GNDDIGITAL — C42 .15 — C41 220UF/16V — C32 .15 — C31 .15 — C35 .15 — C36 220UF/16V — C25 .15 — C30 220UF/16V — +5V — +15V — U13

-30 — C64 3300UF35V — U16 7915 — -15V — GNDANALOG — C63 3300UF35V — +30 — U15 7815 — +15V

U6 790SAVD — -5VD — +15VD — U14 — -5V — U1 — +5VD — +15VD


U3:D
74HC86
U3:C
74HC86
GNDDIGITAL
+5VD
+15D
U2
R7
22.1
V+AN
C12
.1
R6
100K
POLARITY
74HC86
U3:B
POLARITY SWITCH WITH HC86
+5VD
R8
100K
74HC86
U3:A
EMP
LOW=EMP
C11 .1
+5VD
C9
220UF/16V
D2
1N5817
RXP
R5 10
RXN
R4 10
C7
.01PP
C8
.01PP
K2
PAD100
PAD101
PAD102
AES/EBU
TR2
C2 .1
R2
453
D1
1N5817
RXP
RXN
CS8412
U4
CS8412
LOCKL
256/OUT
V+AN
C10
220UF
C13
.1
C14
.047
R9
1K
GNDDIGITAL
CRYSTAL MODE SIX
RIGHT JUST MSB FIRST 18 BITS
REFERENCE 44.1 TO PLL
U5
C15
330PF
EMP
F0
F1
C16
.1UF
OUTPUT FROM VCO DIVIDER
P2:1
P2:2
IDC2X10M
IDC2X10M
F1
F0
256
44.1
GNDDIGITAL
IN2
20VD
K1
RXP
RXN
PAD103
PAD104
RCA/SPDIF
C1 .1
TR1
R1
301
IN1
20VD
RX1
K3
TOSLINK IN
+5VD
R3
22UH
C6
.1
C5
220UF
C4
.1
C3
220UF
IN3
20VD
U1
K4
RXP
RXN
IN4
20VD
P1:1
P1:2
+15D
20VD
POLARITY
256/OUT
IN1
IN2
IN3
IN4
LOCKL
IDC2X10M
IDC2X10M
FIRST RUN SHIPPED
Title
PL55 RECIEIVER BOARD
Size
C
Number
Rev
0
Date
12-11-97
Drawn by Wayne Colburn
Filename
PL55RXR0
Sheet
2
of
4


7805AVID
U3
VOUT
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C3
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R7
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R8
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POLARITY
POWER
D9
D10
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C4
P1:1
P1:2
LOCKL
POLARITY
FS1
FS0
IDC2X10M
IDC2X10M
.1
C6
U1
87C750
RST
R14
10K
C5
4.7UF
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D5
D6
D7
D8
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44.1
48
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R4
150
D1
D2
D3
D4
R1
10K
SW1
INPUT
R2
10K
SW2
POLARITY
150
R3
X1
12MHZ
C1
33PF
C2
33PF
Q1
Q2
Q3
Q4
U2
R13
10K
U4
CLR
CLK
SN74HC4020N
FIRST RUN SHIPPED
Title
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Rev
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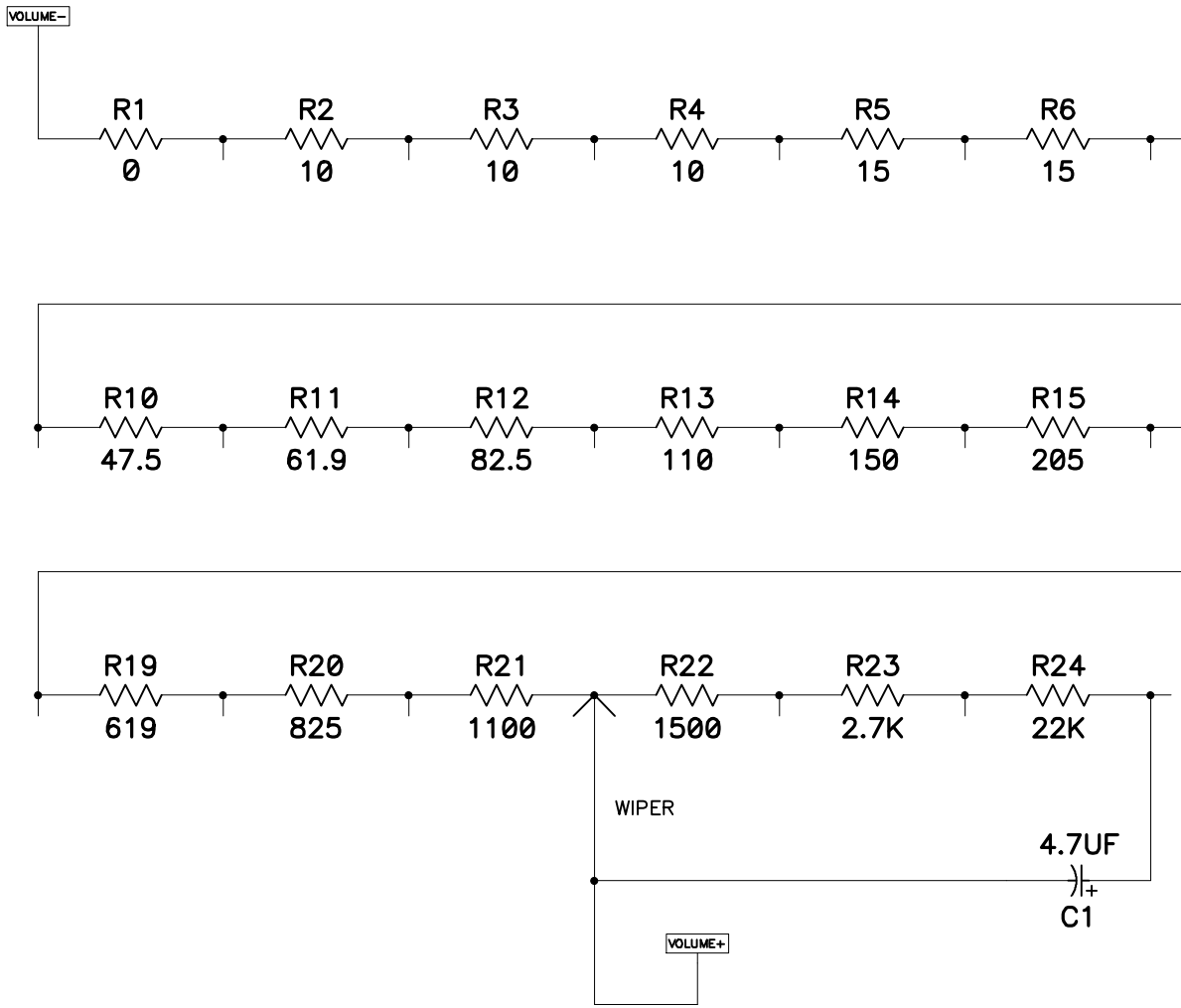
Date
12-11-97
Drawn by WAYNE
Filename
PL55FRTR0.SCH
Sheet 3 of 4



Title	PL55 VOLUME CONTROL	
Size A	Number	Rev 0
Date 12-11-97		Drawn by W C
Filename PL55VOLRO.SCH		Sheet 4 of 4