Applications of the CA3080 High-Performance Operational Transconductance Amplifiers

Application Note | May 2002 | AN6668.2

Author: Hal Wittlinger

Introduction

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply:

$$\text{Transconductance } g_M = \frac{\Delta i_{OUT}}{\Delta e_{IN}}$$

The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Application Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with CMOS devices as post-amplifiers.

Figure 1 shows the equivalent circuit for the OTA. The output signal is a current which is proportional to the transconductance (g_M) of the OTA established by the amplifier bias current (I_{ABC}) and the differential input voltage (e_{IN}). The OTA can either source or sink current at the output terminal, depending on the polarity of the input signal.

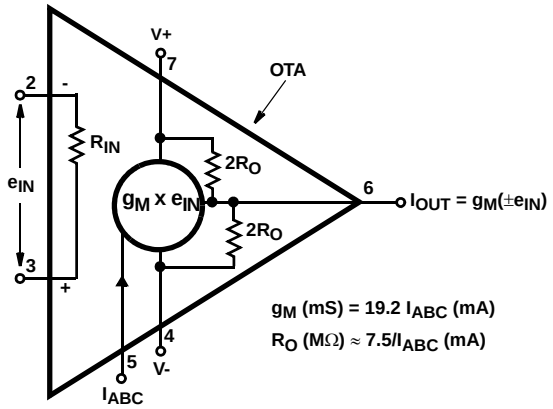


FIGURE 1. BASIC EQUIVALENT CIRCUIT OF THE OTA

The availability of the amplifier bias current (I_{ABC}) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

Circuit Description

A simplified block diagram of the OTA is shown in Figure 2. Transistors Q_1 and Q_2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Figure 3A shows the basic type of current-mirror which is comprised of two transistors, one of which is diode-connected. In a current-mirror with similar geometries for Q_A and Q_B, the current I' establishes a second current I whose value is essentially equal to that of I'.

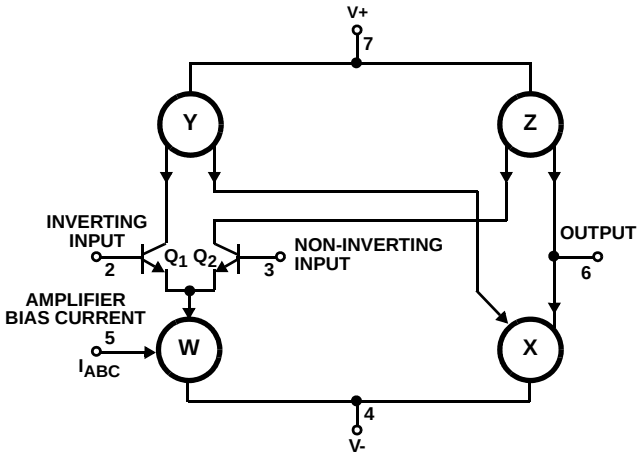


FIGURE 2. SIMPLIFIED DIAGRAM OF THE OTA

This basic current-mirror configuration is sensitive to the transistor beta (β). The addition of another active transistor, shown in Figure 3B, greatly diminishes the circuit sensitivity to transistor beta and increases the current-source output impedance in direct proportion to the transistor beta. Current-mirror W (Figure 2) uses the configuration shown in Figure 3A, while mirrors X, Y, and Z are basically the version shown in Figure 3B. Mirrors Y and Z employ PNP transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes current-mirrors in more detail.

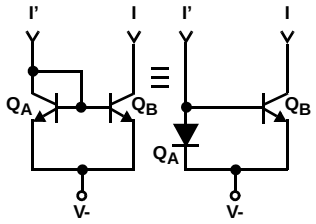


FIGURE 3A. DIODE-CONNECTED TRANSISTOR PAIRED WITH TRANSISTOR

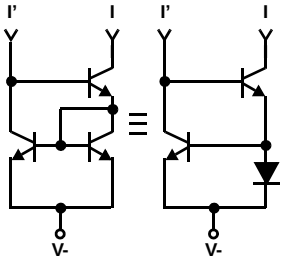


FIGURE 3B. IMPROVED VERSION: EMPLOYS AN EXTRA TRANSISTOR

FIGURE 3. BASIC TYPES OF CURRENT MIRRORS

Figure 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, I_{ABC}, establishes the emitter current of the input differential amplifier Q_1 and Q_2. Hence, effective control of the differential transconductance (g_M) is achieved.

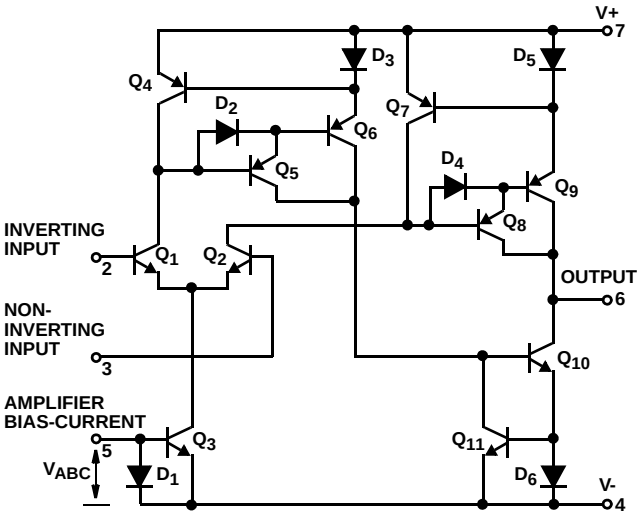


FIGURE 4. SCHEMATIC DIAGRAM OF OTA TYPES CA3080 AND CA3080A

The g_M of a differential amplifier is equal to:

$$\frac{q\alpha I_C}{2KT}$$

(see Reference 2 for derivation) where q is the charge on an electron, α is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), I_C is the collector current of the constant-current source (I_{ABC} in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_M = 19.2 \times I_{ABC}$, where g_M is in mS and I_{ABC} is in milliamperes. The temperature coefficient of g_M is approximately -0.33%/^{0}C (at room temperature).

Transistor Q_3 and diode D_1 (shown in Figure 4) comprise the current mirror "W" of Figure 4. Similarly, transistors Q_7, Q_8 and Q_9 and diode D_5 of Figure 4 comprise the generic current mirror "Z" of Figure 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q_{10}, Q_{11}, and diode D_6 of Figure 4 comprise the current-mirror "X" of Figure 2. Diodes D_2 and D_4 are connected across the base-emitter junctions of Q_5 and Q_8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the "Z" and "X" current-mirror of Figure 2, providing a push-pull Class A output stage that produces full differential g_M. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of g_M and input offset voltage, less variation of input offset voltage with variation of I_{ABC} and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000MΩ.

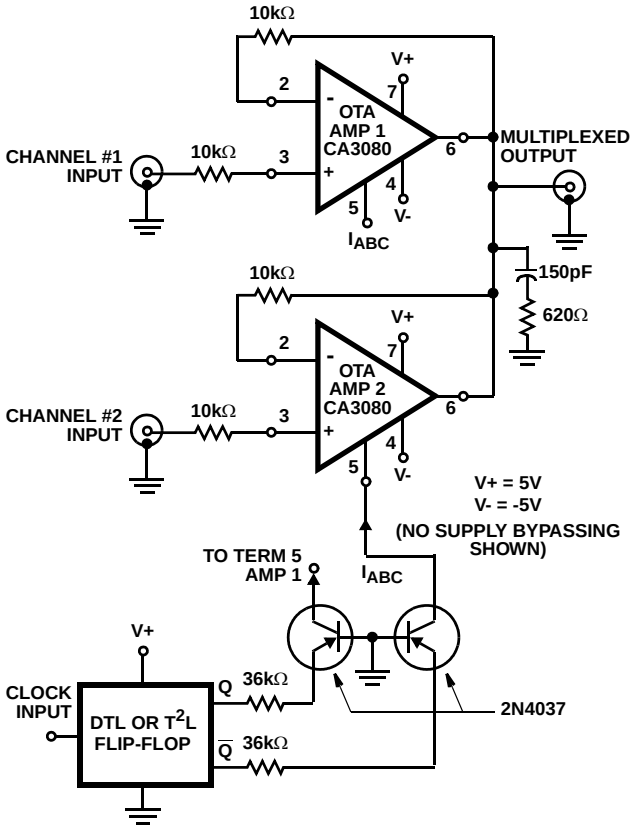


FIGURE 5. SCHEMATIC DIAGRAM OF OTAs IN A TWO-CHANNEL LINEAR TIME-SHARED MULTIPLEXER CIRCUIT

Applications

Multiplexing

The availability of the bias current terminal, I_{ABC}, allows the device to be gated for multiplexer applications. Figure 5 shows a simple two-channel multiplexer system using two CA3080 OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is low. To further increase the gain and reduce the effects of loading, an additioanl buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example ±5V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15V, with the positive-supply at 5V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through PNP transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base configuration is used to minimize capacitive feed-through coupling via the base-collector junction of the PNP transistor.

Another multiplexer system using the OTAs clocked by a CMOS flip-flop is shown in Figure 6. The high output voltage capability of the CMOS flip-flop permits the circuit to be driven directly without the need for PNP level-shifting transistors.

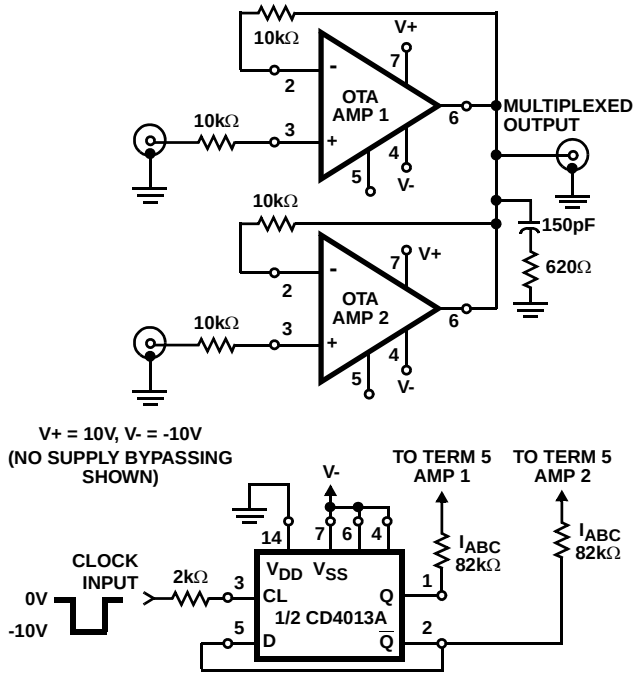
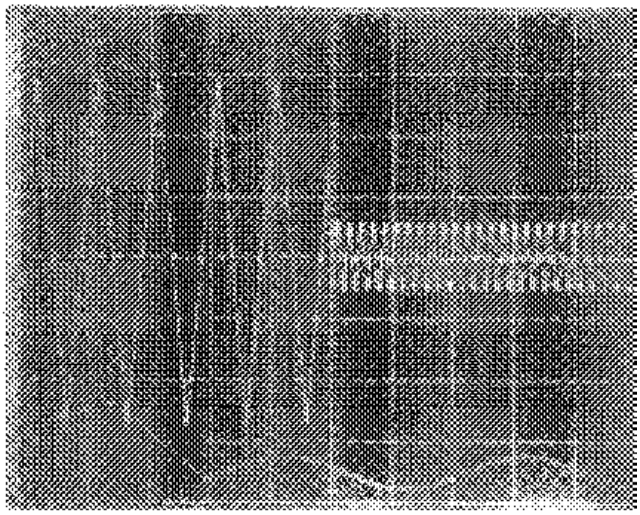


FIGURE 6. SCHEMATIC DIAGRAM OF A TWO-CHANNEL LINEAR MULTIPLEXER SYSTEM USING A CMOS FLIP-FLOP TO GATE TWO OTAs

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figures 5 and 6. The values of the RC-network are chosen so that:

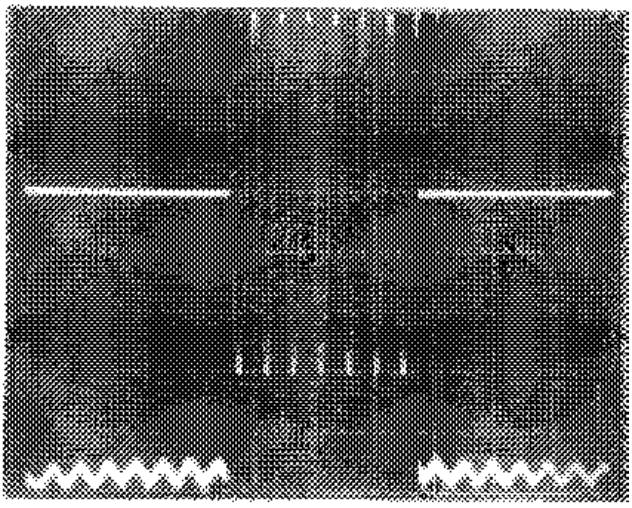
$$\frac{1}{2\pi RC} \cong 2MHz.$$

This RC network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Figure 7 shows an oscilloscope photograph of the multiplexer circuit functioning with two input signals. Figure 8 shows an oscilloscope photograph of the output of the multiplexer with a $6V_{P-P}$, sine wave signal (22kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80dB between channels.



Top Trace: Multiplexed Output; 1V/Div., 100µs/Div.
Bottom Trace: Time Expansion of Switching Between Inputs; 2V/Div., 5µs/Div.

FIGURE 7. VOLTAGE WAVEFORMS FOR CIRCUIT OF FIGURE 6



Top Trace: Output; 1V/Div., 100µs/Div.
Bottom Trace: Voltage Expansion of Output; 1mV/Div., 100µs/Div.

FIGURE 8. VOLTAGE WAVEFORMS FOR CIRCUIT OF FIGURE 6

Sample-and-Hold Circuits

An extension of the multiplex system application is a sample-and-hold circuit (Figure 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Figure 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to “hold” charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000MΩ under cut-off conditions, and the loading on the storage capacitor during the

hold-mode is minimized. An effective solution to the read-out requirement involves the use of a 3N138 insulated-gate field-effect transistor (MOSFET) in the feedback loop. This transistor has a maximum gate-leakage current of 10pA; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Figure 9) is approximately 100dB if the MOSFET is used in the source-follower mode with the CA3080A as the input amplifier. The open-loop output impedance ($1/g_M$) of the 3N138 is approximately 220Ω because its transconductance is about 4,600μS at an operating current of 5mA. When the CA3080A drives the 3N138, the closed loop operational-amplifier output impedance characteristic is:

$$Z_{OUT} \cong \frac{Z_O(\text{OPEN-LOOP})}{A(\text{OPEN-LOOP VOLTAGE-GAIN})}$$

$$\cong \frac{220\Omega}{100\text{dB}} \cong \frac{220\Omega}{10^5} \cong 0.0022\Omega$$

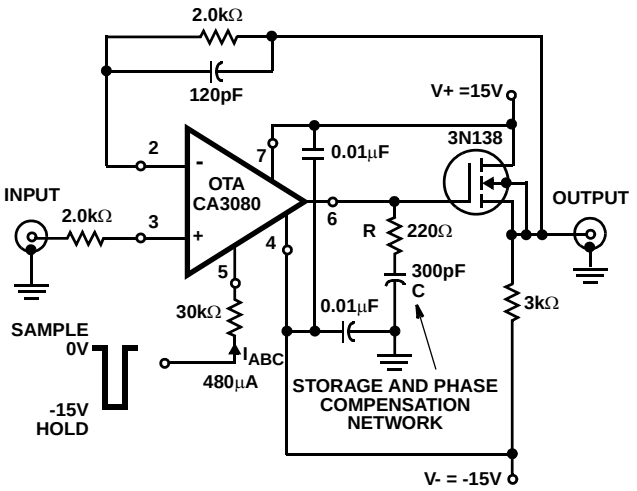
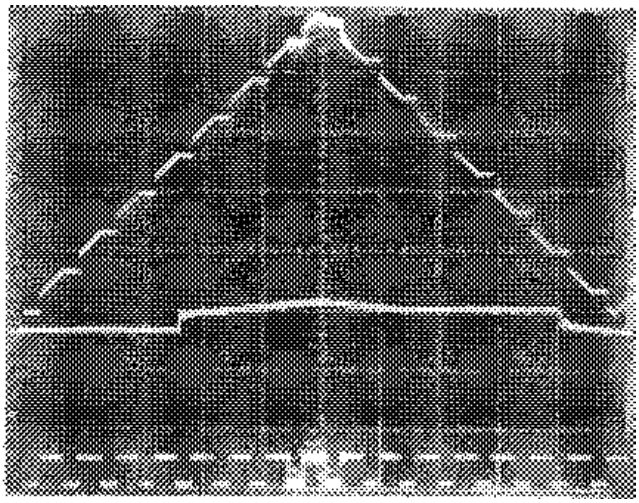


FIGURE 9. SCHEMATIC DIAGRAM OF OTA IN A SAMPLE-AND-HOLD CIRCUIT

Figure 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular waveform. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2μs/Div.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5nA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Figure 11 shows the expected pulse "tilt" in microvolts versus time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50nA, 5nA, 500pA.



Top Trace: Sampled Signal 1V/Div., 20μs/Div.
Center Trace: Top Portion of Upper Signal; 1V/Div., 2μs/Div.
Bottom Trace: Sampling Signal; 20V/Div., 20μs/Div.

FIGURE 10. WAVEFORMS FOR CIRCUIT OF FIGURE 9

Figure 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14ms with a 300pF storage capacitor. The center trace (expanded to 20mV/Div.) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170pA (I = C dv/dt).

Figure 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Figure 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Figure 13 were recorded with supply voltages of ±10V and the series input resistor at terminal 5 was 22kΩ.

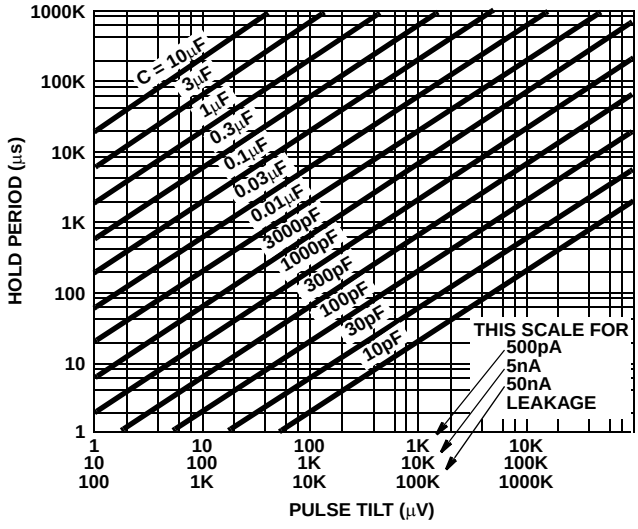
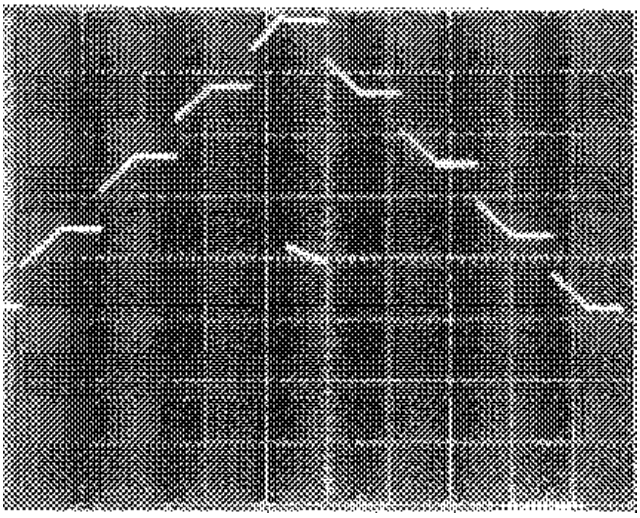
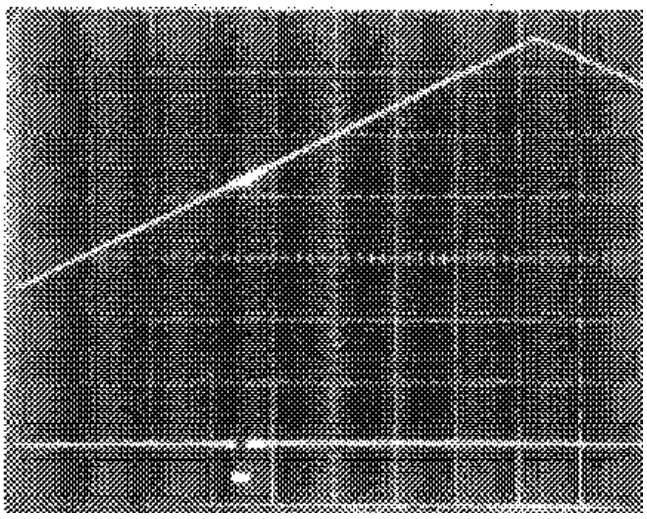


FIGURE 11. "TILT" IN "HELD" VOLTAGE vs HOLD TIME



Top Trace: Sampled Signal; 1V/Div., 20ms/Div.
Center Trace: Worse Case Tilt; 20mV/Div., 20ms/Div.

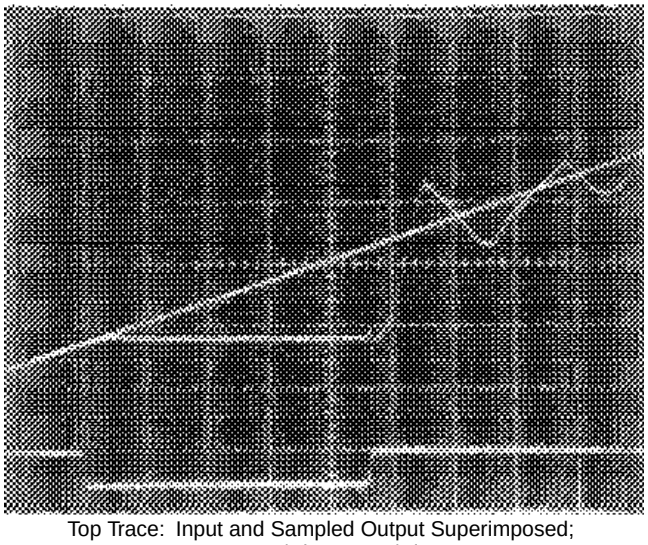
FIGURE 12. "TRIANGULAR-VOLTAGE" BEING SAMPLED BY CIRCUIT OF FIGURE 9



Top Trace: Input and Output Superimposed; 1V/Div., 2μs/Div.
Bottom Trace: Sampling Signal; 20V/Div., 2μs/Div.

FIGURE 13. "RAMP-VOLTAGE" BEING SAMPLED BY CIRCUIT OF FIGURE 9

In Figure 14, the trace of Figure 13 has been expanded (100mV/Div. and 100ns/Div.) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1μs. The resistor in series with the 300pF phase-compensation capacitor was adjusted to 68Ω for minimum recovery time.



Top Trace: Input and Sampled Output Superimposed; 100mV/Div., 100ns/Div.
Bottom Trace: Sampling Signal; 20V/Div., 100ns/Div.

FIGURE 14. "TRIANGULAR-VOLTAGE" BEING SAMPLED BY CIRCUIT OF FIGURE 9

Figure 15 shows the basic circuit of Figure 9 implemented with a 2N4037 PNP transistor to minimize capacitive feedthrough. Figure 16 shows oscilloscope photographs taken with the circuit of Figure 15 operating in the sampling mode at supply voltage of ±15V. The 9.1kΩ resistor in series with the PNP transistor emitter establishes amplifier-bias-current (I_{ABC}) conditions similar to those used in the circuit of Figure 9.

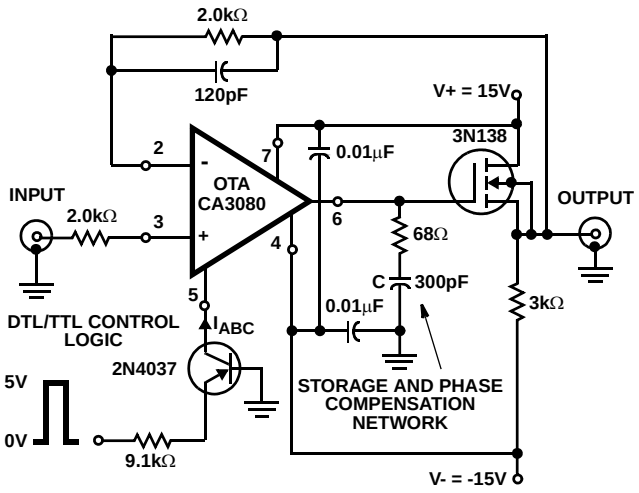
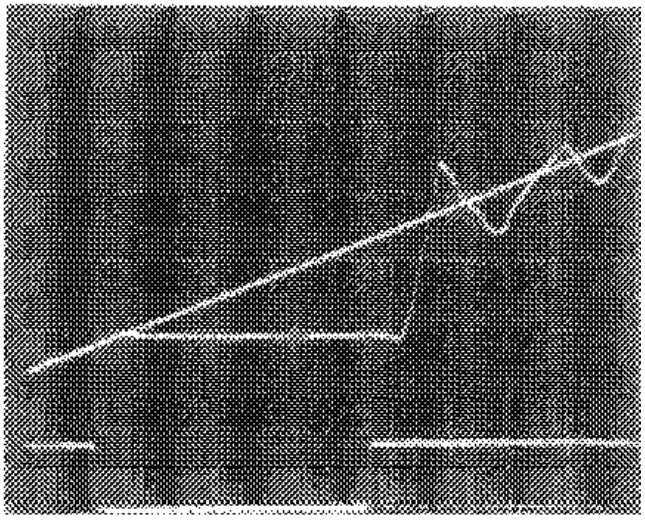


FIGURE 15. SCHEMATIC DIAGRAM OF THE OTA IN A SAMPLE-AND-HOLD CONFIGURATION (DTL/TTL CONTROL LOGIC)



Top Trace: Input and Sampled Output Superimposed; 100mV/Div., 100ns/Div.
Bottom Trace: Sampling Signal; 5V/Div., 100ns/Div.

FIGURE 16. CIRCUIT OF FIGURE 15 OPERATING IN SAMPLING MODE

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $1/2\pi RC \cong 2MHz$, corresponding to the first pole in the amplifier at an output current level of 500μA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figures 9 and 15. The 120pF capacitor shunting the 2kΩ resistor improves the amplifier transient response.

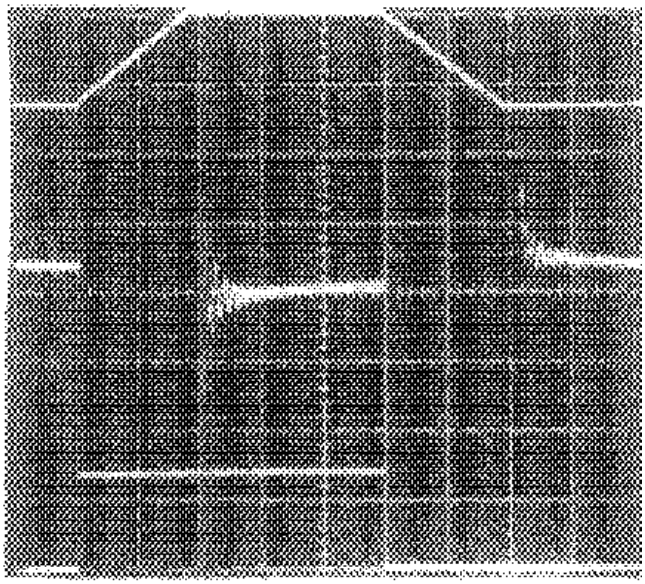
Figure 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Figure 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dv/dt) = 1.8V/μs.

The center trace in Figure 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2mV/Div. The output of the amplifier system settles to within 2mV (the offset voltage specification for the CA3080A) of the input level in 1μs after slewing.

Figure 18 is a curve of slew-rate versus amplifier-bias-current (I_{ABC}) for various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current (I_{ABC}) when the OTA is supplying its maximum output current.

Gain Control - Amplitude Modulation

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current (I_{ABC}) in the OTA because its g_M is directly proportional to the amplifier-bias-current (I_{ABC}). For a specified value of amplifier-bias-current, the output current (I_O) is equal to the product of g_M and the input signal magnitude. The output voltage swing is the product of output current (I_O) and the load resistance (R_L).



Top Trace: Output; 5V/Div., 2μs/Div.
Center Trace: Differential Comparsion of Input and Output; 2mV/Div., 0V thru Center; 2μs/Div.
Bottom Trace: Input; 5V/Div., 2μs/Div.

FIGURE 17. CIRCUIT OF FIGURE 9 OPERATING IN THE LINEAR SAMPLE MODE

Figure 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current (I_O) is equal to $-g_M \times V_X$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, I_{ABC}. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current (I_{ABC}) through resistor R_M. Amplitude modulation of the carrier frequency occurs because variation of the voltage V_M forces a change in the amplifier-bias-current (I_{ABC}) supplied via resistor R_M. When V_M goes positive, the bias current increases which causes a corresponding increase in the g_M of the OTA. When the V_M goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the g_M of the OTA.

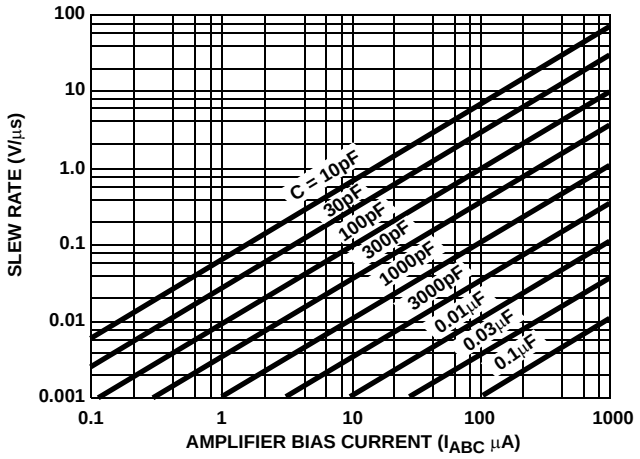


FIGURE 18. SLEW RATE vs AMPLIFIER-BIAS-CURRENT (I_{ABC})

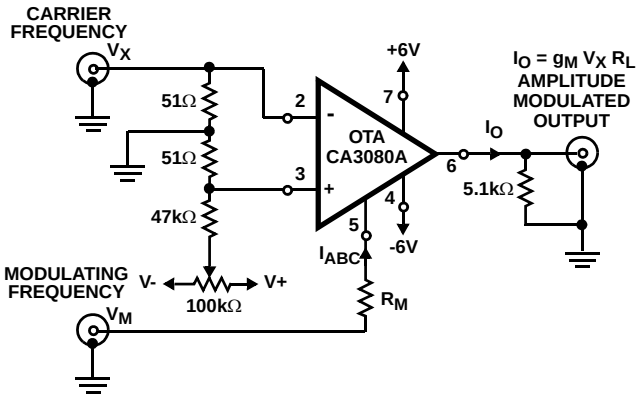


FIGURE 19. AMPLITUDE MODULATOR CIRCUIT USING THE OTA

As discussed earlier, g_M = 19.2 x I_{ABC}, where g_M is in millisiemens when I_{ABC} is in milliamperes. In this case, I_{ABC} is approximately equal to:

$$\frac{V_M - (V\text{-})}{R_M} = I_{ABC}$$

$$I_O = -g_M V_X$$

$$g_M V_X = (19.2)(I_{ABC})(V_X)$$

$$I_O = \frac{-19.2[V_M - (V\text{-})]V_X}{R_M}$$

$$I_O = \frac{19.2(V_X)(V\text{-})}{R_M} - \frac{19.2(V_X)(V_M)}{R_M}$$

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of V_M and the second term represents the modulation, which either adds to or subtracts from the first term. When V_M is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term,

$$(19.2)(V_X)\frac{V_{ABC}}{R_M}$$

involving the amplifier-bias-current terminal voltage (V_{ABC}) (see Figure 4 for V_{ABC}) was neglected. This term was assumed to be small because V_{ABC} is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a PNP transistor), the effect of V_{ABC} variation is eliminated and transferred to the involvement of the PNP transistor base-emitter junction characteristics. Figure 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation.

If an NPN transistor is added to the circuit of Figure 20 as an emitter-follower to drive the PNP transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the NPN base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Figure 21 shows a configuration using one transistor in the CA3018A NPN transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter followers.

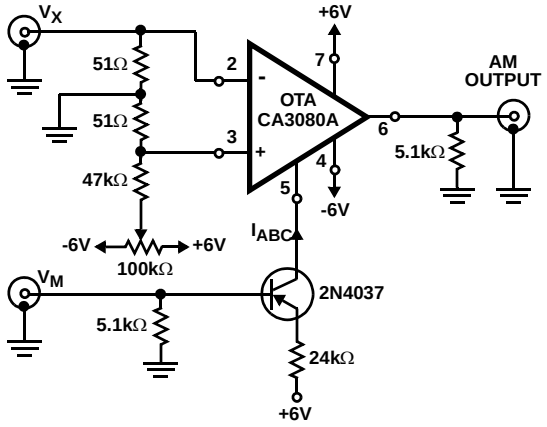


FIGURE 20. AMPLITUDE MODULATOR USING OTA CONTROLLED BY PNP TRANSISTOR

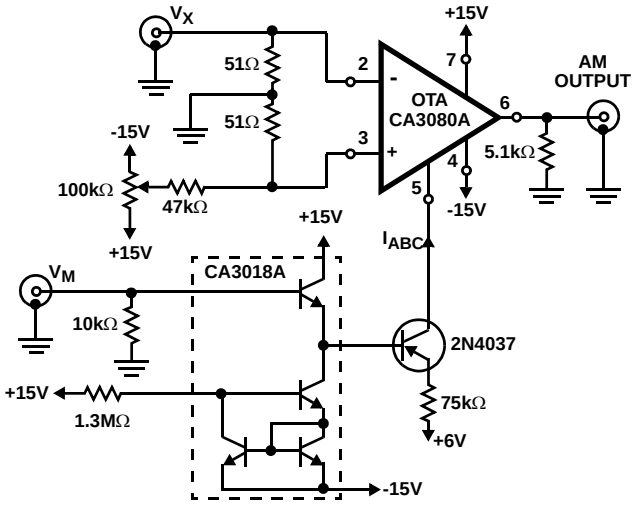


FIGURE 21. AMPLITUDE MODULATOR USING OTA CONTROLLED BY PNP AND NPN TRANSISTORS

The 100kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figures 22A and 22B show oscilloscope photographs of the output voltages obtained when the circuit of Figure 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Figure 22C shows the excellent isolation (>80dB at f = 100kHz) achieved in this modulator during the “gated-off” condition.

Four-Quadrant Multipliers

A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Figure 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy

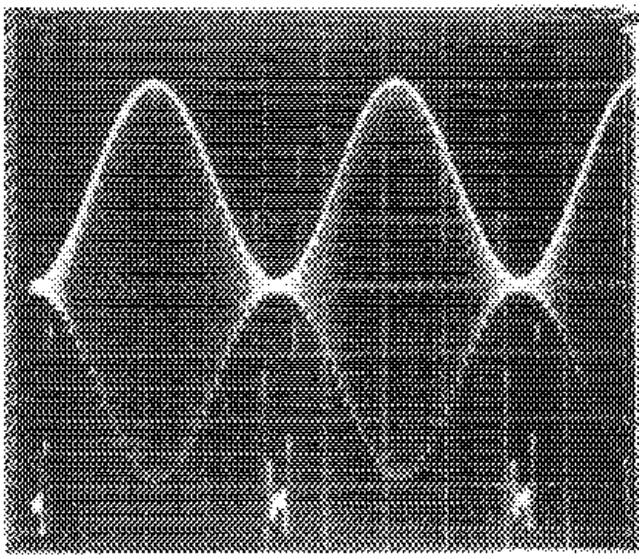
requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Figure 19).

To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_M$. The output current is $I_O = g_M (-V_X)$ because the input is applied to the inverting terminal of the OTA. The output current due to the resistor (R) is V_X/R. Hence, the two signals cancel when $R = 1/g_M$. The current for this configuration is:

$$I_O = \frac{-19.2\ V_X V_M}{R_M}, \text{ and } V_M = V_Y$$

The output signal for these configurations is a current which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter as shown in Figure 24.

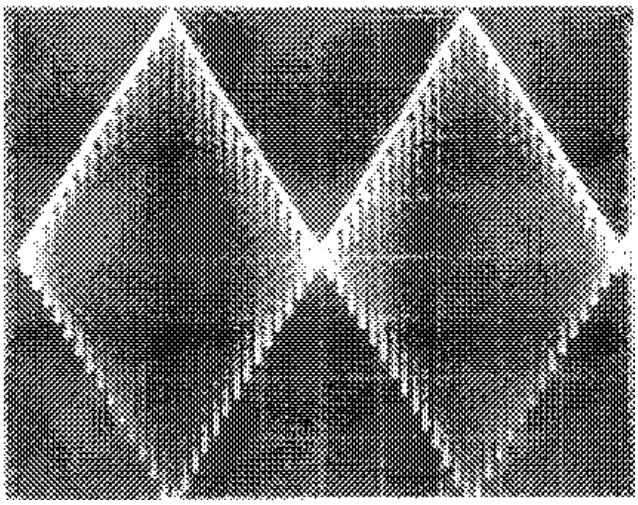
In Figure 23, the current “cancellation” in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).



TIME (50μs/DIV.)

Top Trace: Modulation Input (≅ $20V_{P-P}$)
Center Trace: Amplitude Modulated Output; 500mV/Div.
Bottom Trace: Expanded Output to Show Depth of Modulation; 20mV/Div.

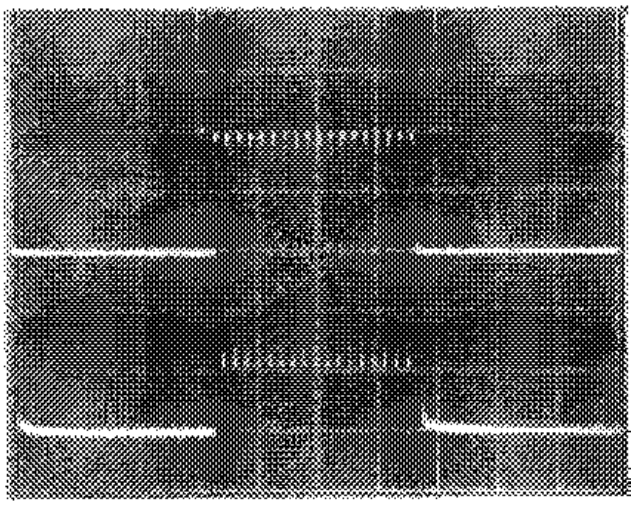
FIGURE 22A. RESPONSE FOR SINE WAVE MODULATION



TIME (50μs/DIV.)

Top Trace: Modulation Input (20V)
Bottom Trace: Amplitude Modulated Output; 500mV/Div.

FIGURE 22B. RESPONSE FOR TRIANGLE WAVE MODULATION



TIME (50μs/DIV.)

Top Trace: Gated Output; 1V/Div.
Bottom Trace: Voltage Expansion Of Above Signal Showing No Residual; 1mv/Div.

FIGURE 22C. RESPONSE FOR SQUARE WAVE MODULATION

FIGURE 22. AMPLITUDE MODULATOR CIRCUIT OF FIGURE 19 WITH $R_M = 40k\Omega$, $V_S = \pm 10V$

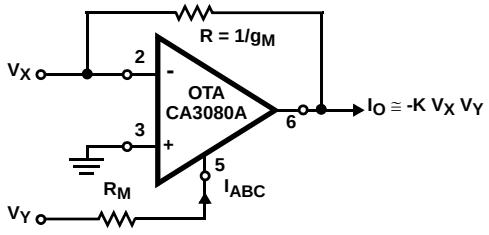


FIGURE 23. BASIC FOUR QUADRANT ANALOG MULTIPLIER USING AN OTA

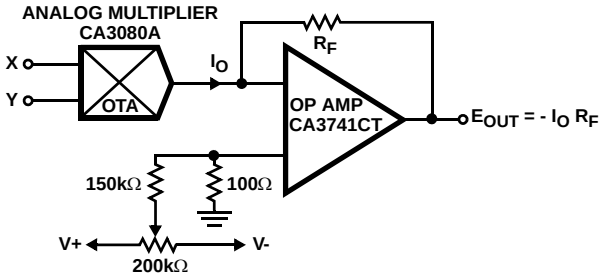


FIGURE 24. OTA ANALOG MULTIPLIER DRIVING A CURRENT-TO-VOLTAGE CONVERTER

Figure 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent full-scale. There are only three adjustments: 1) one is on the output, to compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20kΩ potentiometer establishes the g_M of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

Procedure for adjustment of the circuit:

1. a) Set the 1MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100kΩ potentiometer until a 0V reading is obtained at the output.
2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator (it is essential that a low impedance source be used; this minimizes any change in the g_M balance or zero-point due to the 50μA Y-input bias current).
   b) Adjust the 20kΩ potentiometer in series with Y-input until a reading of 0V is obtained at the output. This adjustment establishes the g_M of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1MΩ resistor for an output voltage of 0V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

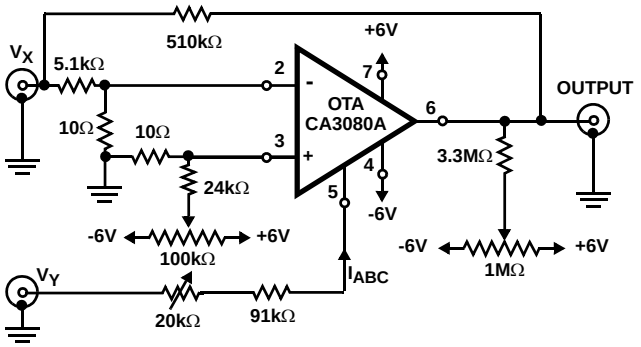


FIGURE 25. SCHEMATIC DIAGRAM OF ANALOG MULTIPLIER USING OTA

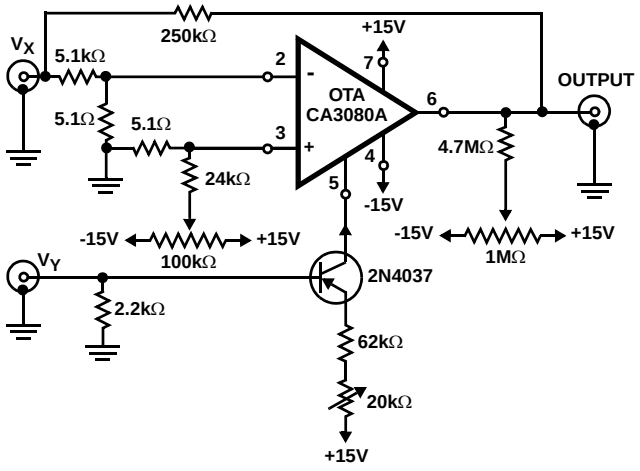
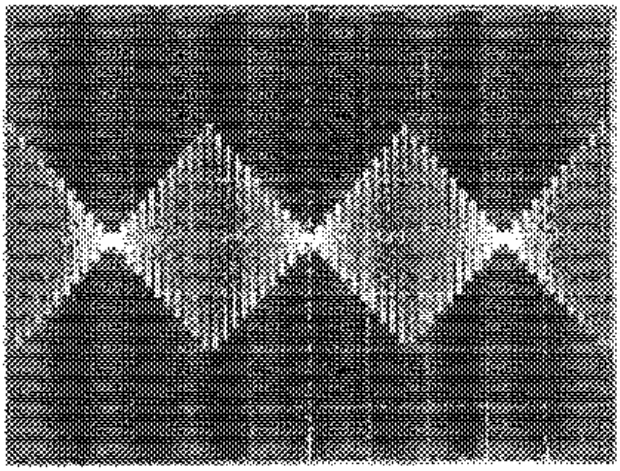


FIGURE 26. SCHEMATIC DIAGRAM OF ANALOG MULTIPLIER USING OTA CONTROLLED BY A PNP TRANSISTOR

Figure 26 shows the schematic of an analog multiplier circuit with a 2N4037 PNP transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the PNP transistor. The addition of another emitter-follower preceeding the PNP transistor (shown in Figure 21) will further increase the current gain while markedly reducing the effect of the V_{be} temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

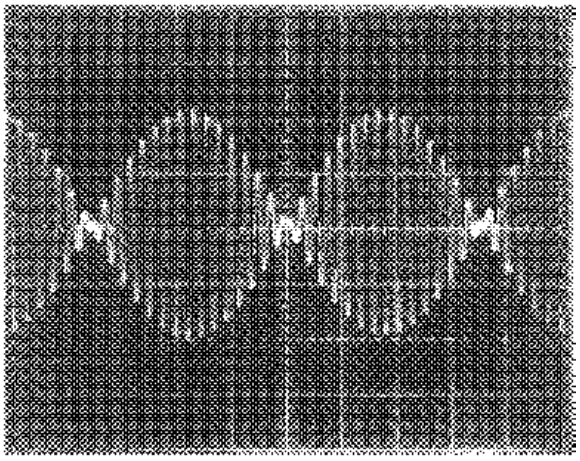
Figures 27A and 27B show oscilloscope photographs of the output signals delivered by the circuit of Figure 26 which is connected as a suppressed-carrier generator. Figures 28A and 28B contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular- wave inputs.

If ±15V power supplies are used (shown in Figure 26), both inputs can accept ±10V input signals. Adjustment of this multiplier circuit is similar to that already described above.



500mV/Div., 200μs/Div.,
Triangular Input: 700Hz; $5V_{P-P}$ to V_Y Input
Carrier Input: 30kHz; $13.5V_{P-P}$ to V_X Input

FIGURE 27A.



500mV/Div., 200µs/Div.,
Modulating Frequency: 700Hz; $5V_{P-P}$ to V_Y Input
Carrier Input: 21kHz; $13.5V_{P-P}$ to V_X Input

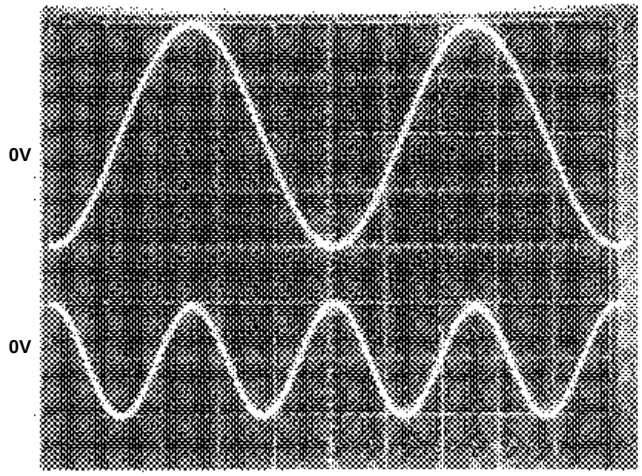
FIGURE 27B.

FIGURE 27. WAVEFORMS OBSERVED WITH OTA ANALOG MULTIPLIER USED AS A SUPPRESSED CARRIER GENERATOR

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

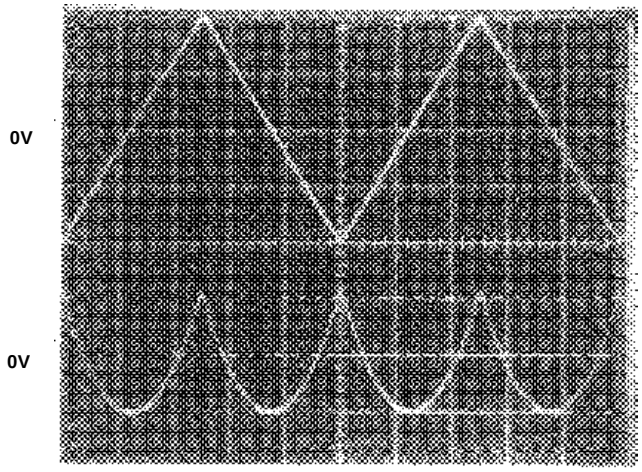
Linear Multiplexer - Decoder

A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Figure 29. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Figure 30 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10µs delay-"one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-hold circuit for approximately 1µs. Figure 31 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10µs "one-shot" to decode a signal.



Top Trace: Input to X And Y; 2V/Div., 1ms/Div. (200Hz)
Bottom Trace: Output; 500mV/Div., 1ms/Div. (400Hz)

FIGURE 28A.



Top Trace: Input to X And Y; 2V/Div., 1ms/Div. (200Hz)
Bottom Trace: Output; 500mV/Div., 1ms/Div. (400Hz)

FIGURE 28B.

FIGURE 28. WAVEFORMS OBSERVED WITH OTA ANALOG MULTIPLIER USED IN SIGNAL-SQUARING CIRCUITS

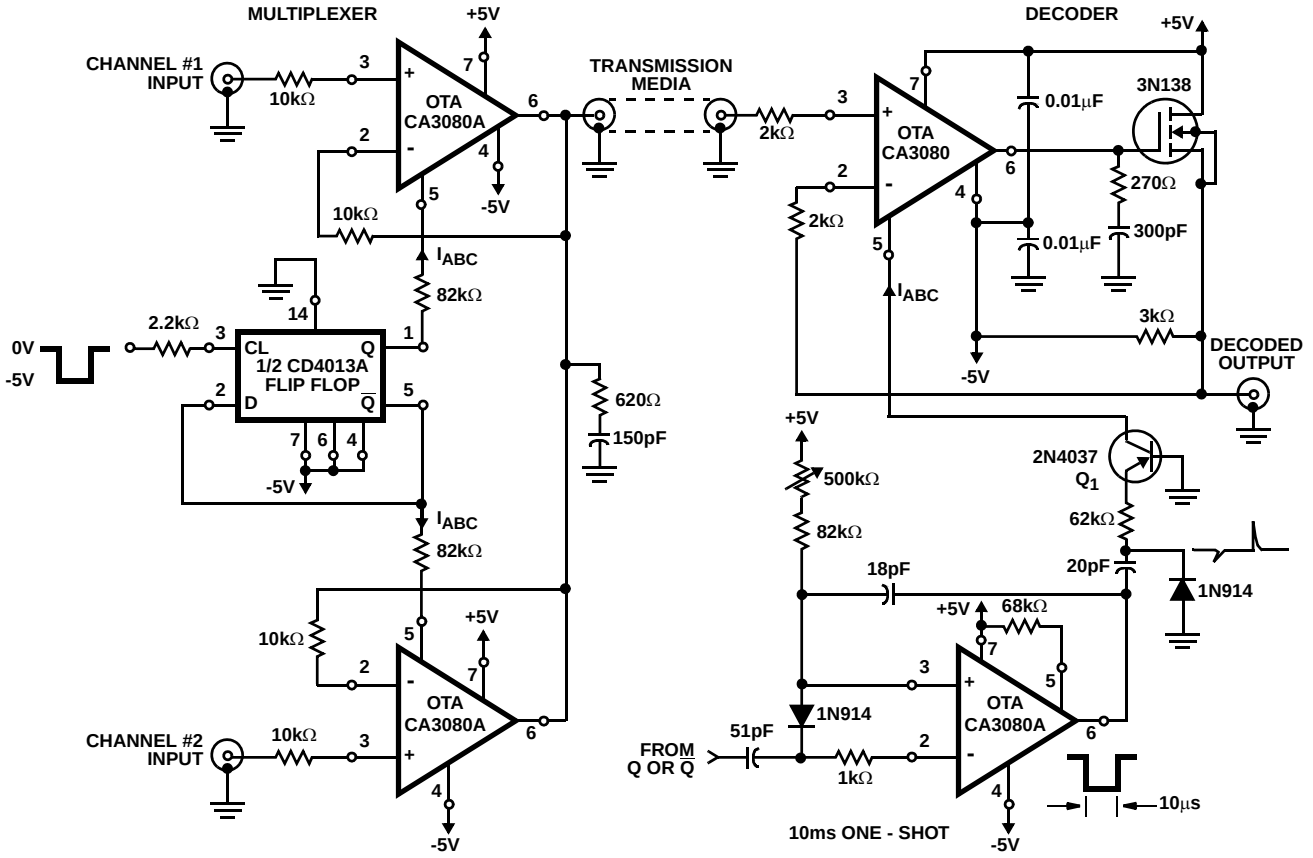
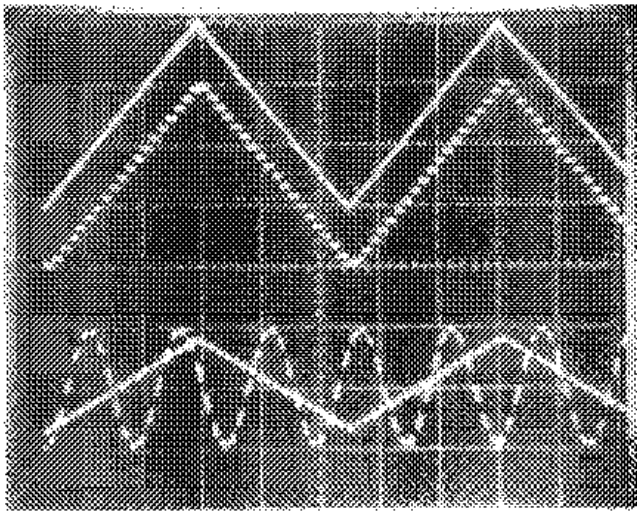
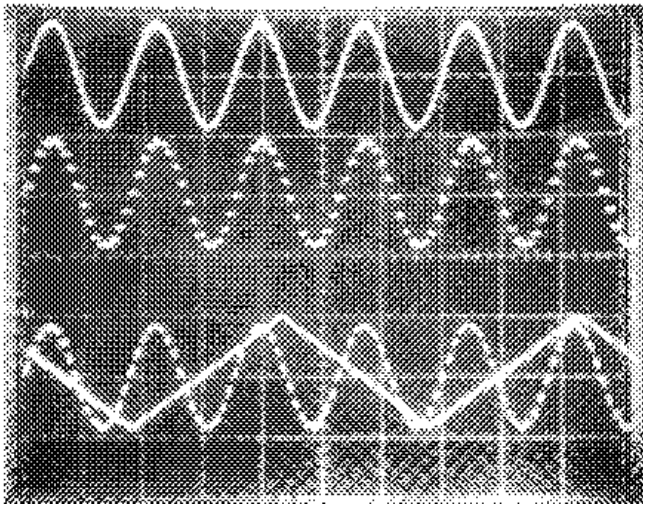


FIGURE 29. TWO-CHANNEL MULTIPLEXER AND DECODER USING OTAs

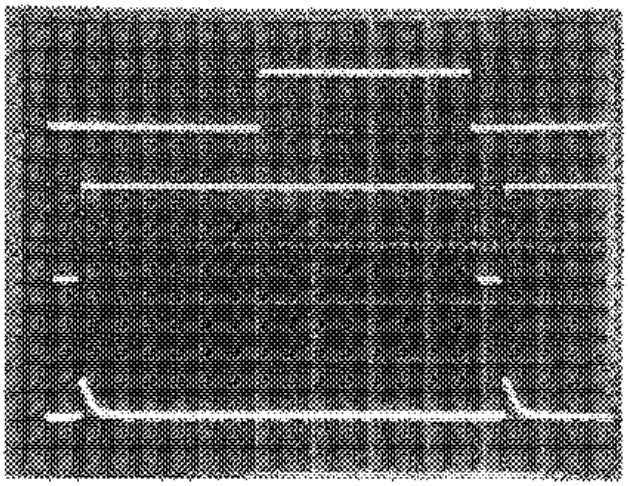


Top Trace: Input Signal; 1V/Div., 20ms/Div.
Center Trace: Recovered Output; 1V/Div., 20ms/Div.
Bottom Trace: Multiplexed Signals; 2V/Div., 20ms/Div.



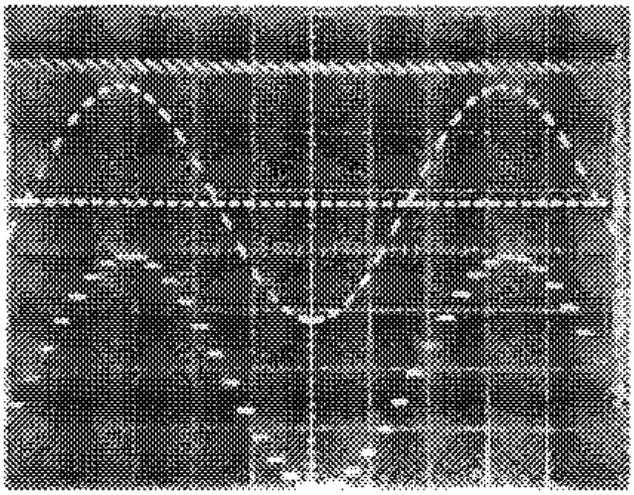
Top Trace: Input Signal; 1V/Div., 20ms/Div.
Center Trace: Recovered Output; 1V/Div., 20ms/Div.
Bottom Trace: Multiplexed Signals; 1V/Div., 20ms/Div.

FIGURE 30. WAVEFORMS SHOWING OPERATION OF LINEAR MULTIPLEXER/SAMPLE-AND-HOLD DECODE CIRCUITRY (FIGURE 29)



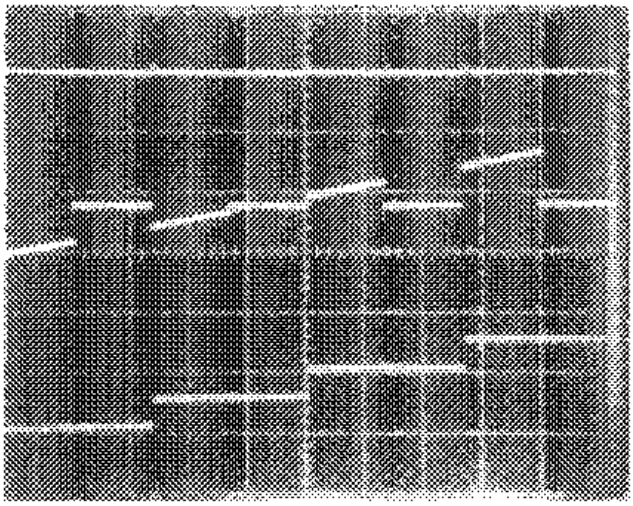
Top Trace: Flip-flop Output; 5V/Div., 20μs/Div.
Center Trace: "One-shot" Output; 5V/Div., 20μs/Div.
Bottom Trace: Strobe Pulse At The Collector of Q_1; 0.1V/Div., 20μs/Div.

FIGURE 31A. WAVEFORMS CONTROLLING DECODER ENABLE



Top Trace: Strobe Pulse at Q_1; 0.5V/Div., 5ms/Div.
Center Trace: Multiplexed Output With One Input at GND; 0.5V/Div., 5ms/Div.
Bottom Trace: Decoded Output; 0.5V/Div., 5ms/Div.

FIGURE 31B. WAVEFORMS SHOWING DECODER OPERATION



500μs/Div.

FIGURE 31C. SAME AS FIGURE 31B BUT WITH EXPANDED TIME SCALE

FIGURE 31. VARIOUS WAVEFORMS SHOWING THE OPERATION OF LINEAR MULTIPLEXER

High-Gain, High-Current Output Stages

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOSFET) shown in Figure 9. This configuration yields a voltage gain equal to the (g_M) (R_O) product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Figure 9) are limited by the 3N138 MOSFET performance and its source-terminal load. In the positive direction, the MOSFET may be driven into saturation; the source-load resistance and the MOSFET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOSFET shown in Figure 9.

Another variation of this generic form of amplifier utilizes the CD4007A (CMOS) inverter as an amplifier driven by the CA3080. Each of the three inverter/amplifiers in the CD4007A has a typical voltage gain of 30dB. The gain of a single CMOS inverter/amplifier coupled with the 100dB gain of the CA3080 yields a total forward-gain of about 130dB. Use of a two-stage CMOS amplifier configuration will increase the total open-loop gain of the system to about 160dB (100,000,000). Figures 32 through 35 show examples of these configurations. Each CMOS inverter/amplifier can sink or source a current of 6mA (Typ). In Figures 34 and 35, two CMOS inverter/amplifiers have been connected in parallel to provide additional output current.

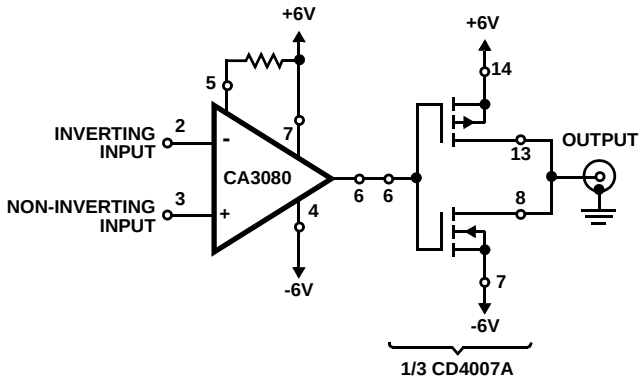


FIGURE 32. OTA DRIVING CMOS INVERTER/AMPLIFIER IN OPEN-LOOP MODE

The open-loop slew-rate of the circuit in Figure 32 is approximately 65V/μs. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1V/μs (shown in Figure 33). Even when the three inverter/amplifiers in the CD4007A are connected as shown in Figure 34, the open-loop slew-rate remains at 65V/μs. A slew-rate of about 1V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Figure 35. Figure 36 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figures 33 and 35. These photos illustrate the inherent stability of the OTA and CMOS circuits operating in concert.

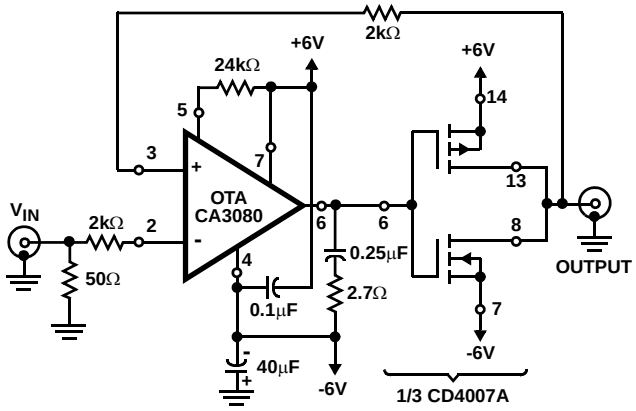


FIGURE 33. OTA DRIVING CMOS INVERTER/AMPLIFIER IN UNITY-GAIN CLOSED-LOOP MODE

Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A CMOS inverter/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figures 32, 33, 34, and 35, for example, power-supply current drawn by the CMOS inverter/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

Figure 37 shows a variety of circuits that can be assembled using the CA3080 to drive one inverter/amplifier in the

CD4007A. For greater output current capability, the remaining amplifiers in the CD4007A may be connected in parallel with the single stage shown. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs power consumption trade-offs may be made by adjustment of the I_{ABC} current to the CA3080. The quiescent power consumption of the circuits shown in Figure 37 is typically 6mW, but can be made to operate in the micropower region by suitable circuit modifications.

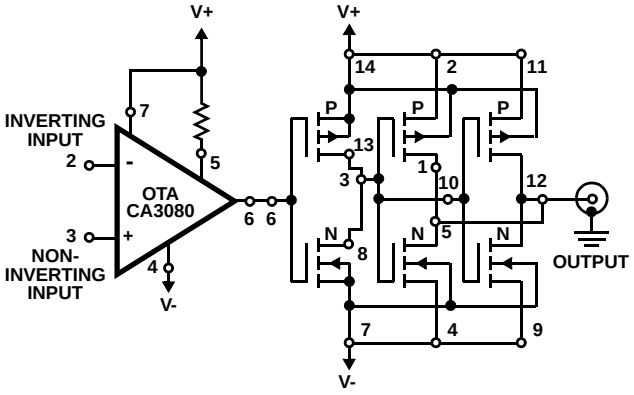


FIGURE 34. OTA DRIVING TWO-STAGE CMOS INVERTER/AMPLIFIER IN OPEN-LOOP MODE

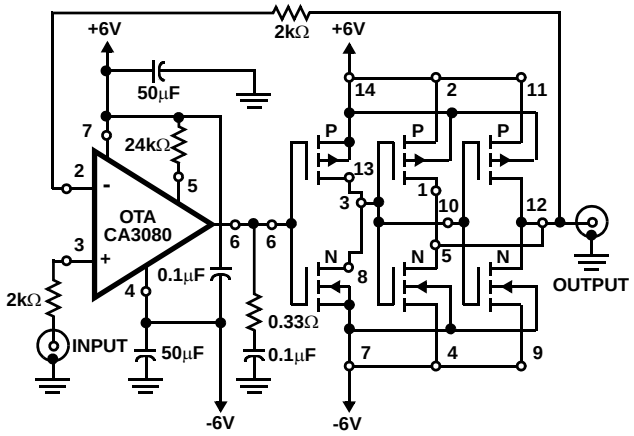
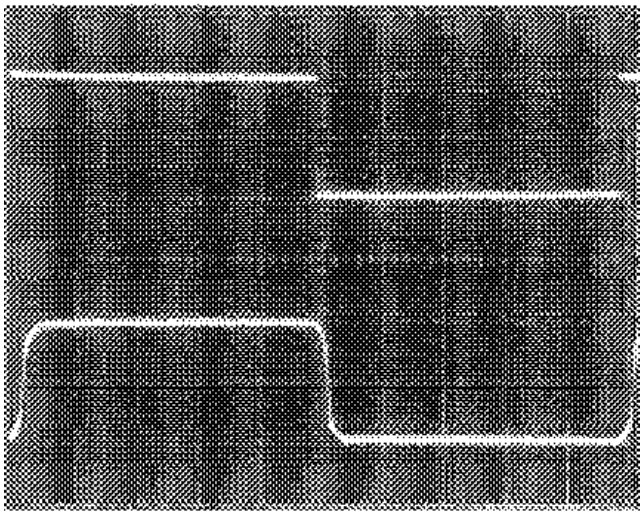
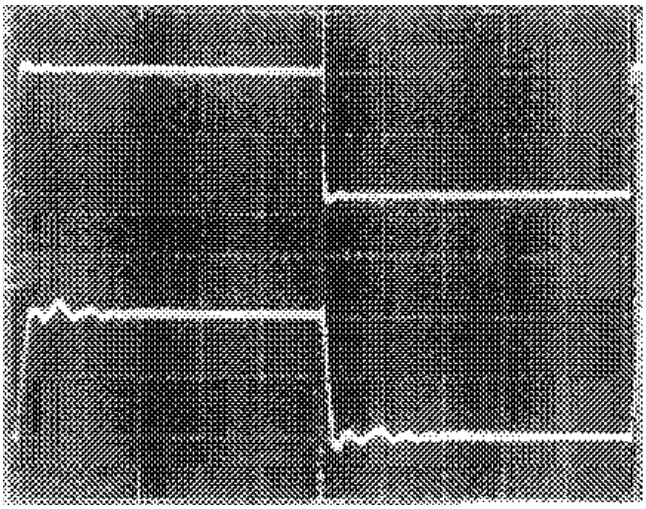


FIGURE 35. OTA DRIVING TWO-STAGE CMOS INVERTER/AMPLIFIER IN UNITY GAIN CLOSED-LOOP MODE



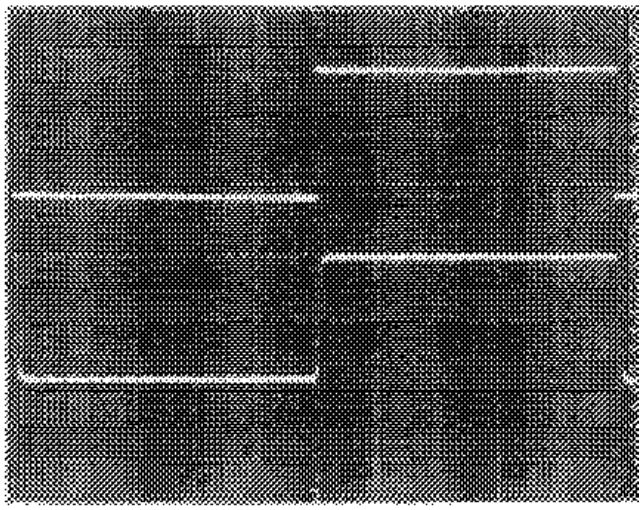
Top Trace: Input; 5V/Div., 100µs/Div.
Bottom Trace: Output; 5V/Div., 100µs/Div.

FIGURE 36A. LARGE SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 33



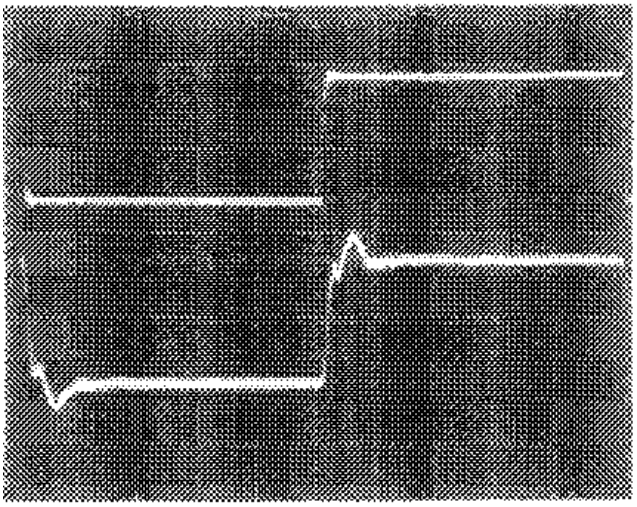
Top Trace: Input; 50mV/Div., 1µs/Div.
Bottom Trace: Output; 50mV/Div., 1µs/Div.

FIGURE 36B. SMALL SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 33



Top Trace: Input; 5V/Div., 100µs/Div.
Bottom Trace: Output; 5V/Div., 100µs/Div.

FIGURE 36C. LARGE SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 35



Top Trace: Input; 50mV/Div., 1µs/Div.
Bottom Trace: Output; 50mV/Div., 1µs/Div.

FIGURE 36D. SMALL SIGNAL RESPONSE FOR CIRCUIT IN FIGURE 35

FIGURE 36. PERFORMANCE OF OTA DRIVING CMOS INVERTER/AMPLIFIER

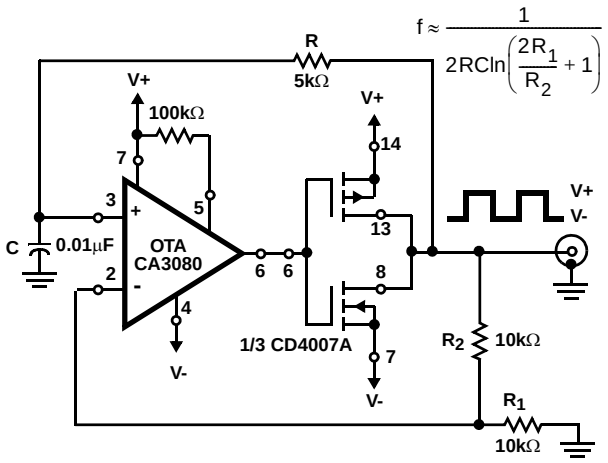


FIGURE 37A. ASTABLE MULTIVIBRATOR

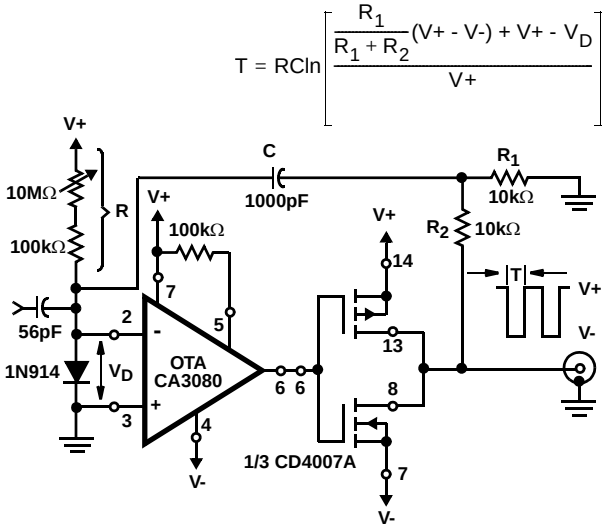


FIGURE 37B. MONOSTABLE MULTIVIBRATOR

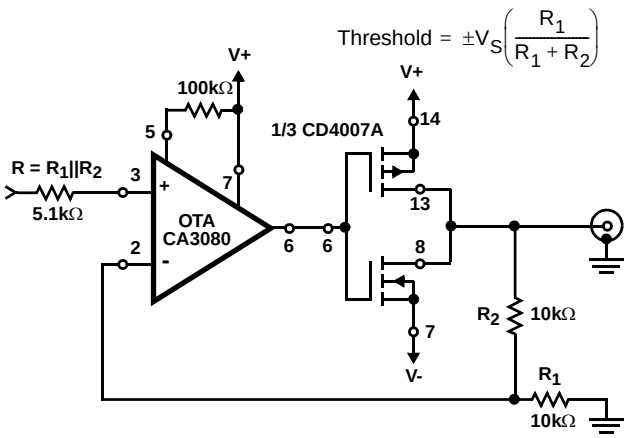


FIGURE 37C. THRESHOLD DETECTOR

FIGURE 37D. MULTISTABLE CIRCUITS USING THE OTA AND CMOS INVERTER/AMPLIFIERS

Micropower Comparator

The schematic diagram of a micropower comparator is shown in Figure 38. Quiescent power consumption of this circuit is about 10μW (Typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420μW. Under these conditions, the circuit responds to a differential input signal in about 8μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150ns, but the power consumption rises to 21mW.

The differential amplifier input common-mode range for the circuit of Figure 38 is -1V to +10.5V. Voltage gain of the micropower comparator is typically 130dB. For example, a 5μV input signal will switch the output.

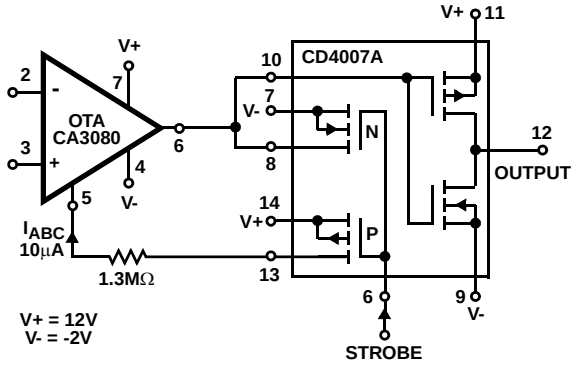


FIGURE 37. SCHEMATIC DIAGRAM OF MICROPOWER COMPARATOR USING THE CA3080A AND CMOS CD4007A

Appendix I

Current Mirrors

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Figure A shows this basic configuration of the current-mirror. Q_2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta I_B$. If a current I_1 is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q_2 such that Q_2 "sinks" the applied current I_1.

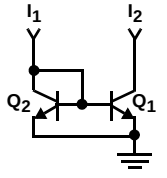


FIGURE 38A. DIODE - TRANSISTOR CURRENT SOURCE

If the base of a second transistor (Q_1) is connected to the base-to-collector junction of Q_2, shown in Figure 39A, Q_1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q_2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current (I_1) and the collector current (I_2) of transistor Q_1, is due to the fact that the base-current for both transistors is supplied from I_1. Figure 39B shows this current division, using a "unit" of base current (1) to each transistor base. This base current causes a collector current to flow in direct proportion to the β of each transistor. The ratio of the "sinking" current I_2 to the input current I_1 is therefore:

$$\frac{I_2}{I_1} = \beta/(\beta + 2).$$

Thus, as β increases, the output current (I_2) approaches the input current (I_1). The curves in Figure 39C show this ratio as a function of the transistor β. When the transistor β is equal to 100, for example, the difference between the two currents is only two percent.

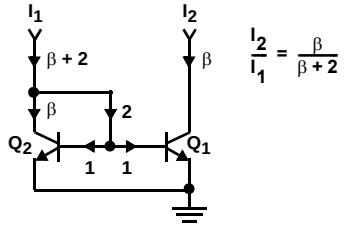


FIGURE 38B. DIODE - TRANSISTOR CURRENT SOURCE. ANALYSIS OF CURRENT FLOW

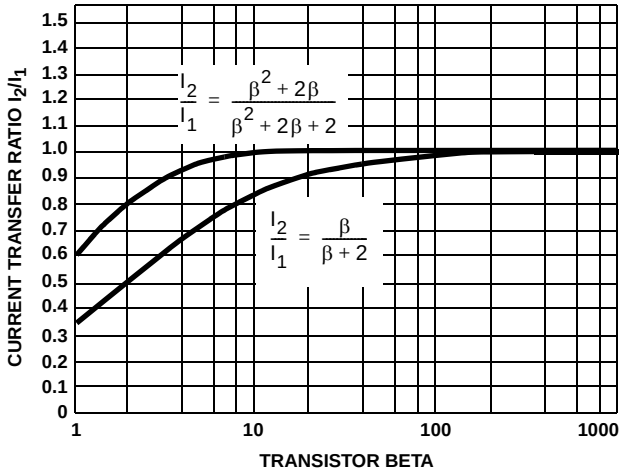
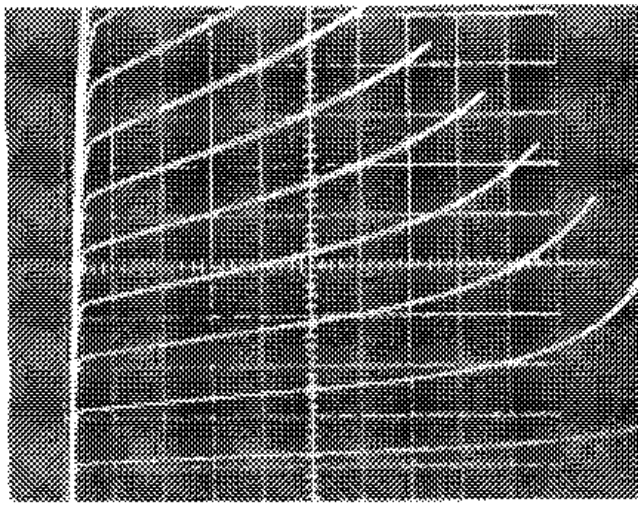


FIGURE 38C. CURRENT TRANSFER RATIO I_2/I_1 vs TRANSISTOR BETA

Figure 39D shows a curve-tracer photograph of characteristics for the circuit of Figure 39B. No consideration in this discussion is given to the variation of the transistor (Q_1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q_1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q_1.



Scale: Horizontal = 2V/Div.
Vertical = 1mA/Div.
Steps = 1mA/STEP

FIGURE 38D. PHOTO SHOWING RESULTS OF FIGURE 39B

This diode-connected transistor (Q_3 in Figure 39E) may be considered as a current-sampling diode that senses the emitter-current of Q_1 and adjusts the base current Q_1 (via Q_2) to maintain a constant-current in I_2. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Figure 39F shows the improved output resistance characteristics of the circuit of Figure 39E. (Compare Figure 39D and 39F).

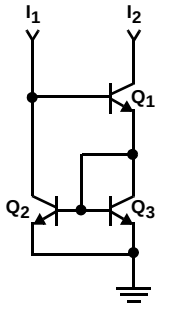
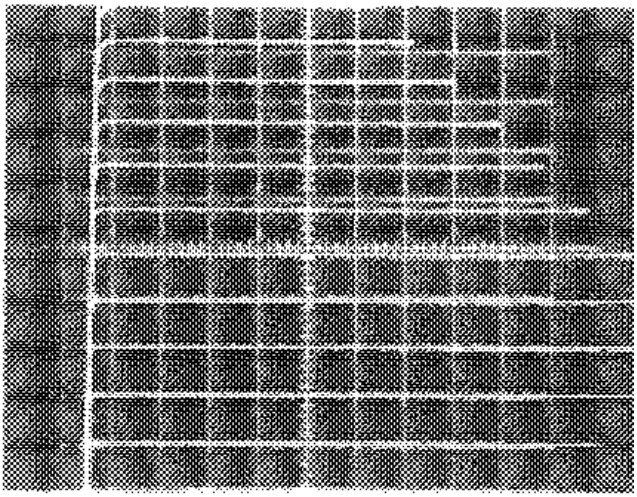


FIGURE 38E. DIODE - 2 TRANSISTOR CURRENT SOURCE



Scale: Horizontal = 2V/Div.
Vertical = 1mA/Div.
Steps = 1mA/STEP

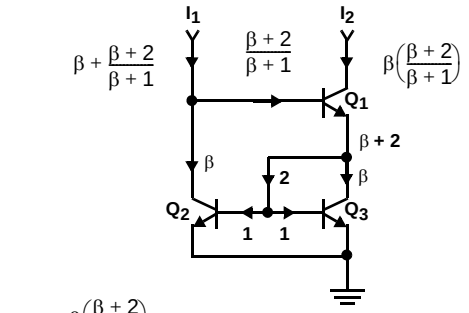
FIGURE 38F. PHOTO SHOWING RESULTS OF FIGURE 39E

Figure 39G shows the current-division within the mirror assuming a “unit” (1) of current in transistors (Q_2 and Q_3).

The resulting current transfer ratio

$$I_2/I_1 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}.$$

Figure 39C shows this equation plotted as a function of beta. It is significant that the current transfer ratio (I_2/I_1) is improved by the β^2 term, and reduces the significance of the $2\beta + 2$ term in the denominator.



$$\frac{I_2}{I_1} = \frac{\beta\left(\frac{\beta + 2}{\beta + 1}\right)}{\beta + \left(\frac{\beta + 2}{\beta + 1}\right)} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$$

FIGURE 38G. CURRENT FLOW ANALYSIS OF FIGURE 39E

Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplication, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with CMOS ICs being operated in the linear mode.

Acknowledgments

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.