Handy S/PDIF Checker

a Digital Audio test unit

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Audio equipment with digital signal interfaces offer high quality sound but trying to listen to what is happening at the interface is not easy without specialised test equipment. A new S/PDIF decoder chip with built-in D/A converters forms the heart of this simple but useful piece of test kit.

The S/PDIF audio digital interface standard has been around for a few years now and is increasingly being adopted by the latest models of CD players, DAT recorders and mini disc systems. Trouble-shooting digital systems invariably calls for the use of expensive test gear to analyse the signals. This circuit idea offers a simple low-cost method of listening-in to the digital interface.

This design uses just one 28-pin SMD chip that together with a voltage regulator and a few passive components produces a useful S/PDIF interface tester. The IC in question is the recently introduced IEC-958 Audio DAC type UDA1350ATS or UDA1351TS from Philips. The block diagram of this IC is shown in **Figure 1** it contains an IEC958 decoder and integrated stereo D/A converters to generate stereo analogue audio output signals from the S/PDIF digital data stream. The UDA1350ATS is an extremely versatile device and to use all the available functions an external microcontroller can be connected via the serial L3 interface, alternatively the chip can be operated in static stand-alone mode by pulling the SELSTATIC input high. In this mode it is not possible to use all the features of the chip such as volume, bass and treble boost, AF filter selection, soft muting or external de-emphasis control but in our application here we are not too concerned about using all the available bells and whistles so the chip is configured in its stand-alone mode.

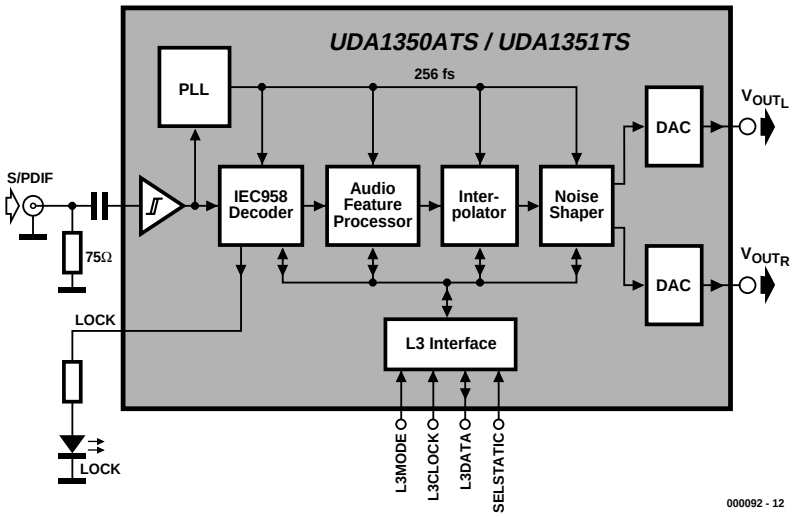

Figure 1. The UDA1350/1 block diagram

Table 1.

Technical data of the UDA 1350 ATS and UDA 1351 TS

Parameter	Value
Operating voltage	+2.7 to +3.6 V
Supply current	80 mW @ 48 kHz 110 mW @ 96 kHz
Vref	0.45 - 0.55 V_{DDA}
Input signal level	0.2 - 3.3 V_{pp}
Input hysteresis	40 mV
Sample rate UDA 1350 ATS	28 kHz - 54 kHz
Sample rate UDA 1351 TS	28 kHz - 100 kHz
Output signal	900 mV_{eff}
Signal/Noise ratio	100 dB typ.
Channel separation	96 dB typ.
Output signal difference	0.1 dB typ.

Signal flow in the UDA1350/1

The digital data stream enters the chip at the

The S/PDIF signal format

Historical perspective

When audio equipment began using digital techniques to store analogue signals (CD players and DAT recorders) the output from the equipment were standard analogue signals. It wasn't long before it was realised that there would be many benefits if the digital audio information were sent between equipment rather than converting to analogue, especially in the professional (studio) environment. The Audio Engineering Society together with The European Broadcasting Union collaborated on a paper outlining a standard for such a digital interface. The EBU-Document Tech. 3250 from November 1985 defined an interface with a 48 kHz (or 32 kHz) sampling frequency and an audio format of 24 bits per channel. Not long after this the electronics companies Sony and Philips jointly specified a consumer version of this interface standard called the S/PDIF (Sony/Philips Digital Interface Standard). The two standards, the professional AES/EBU and the Consumer S/PDIF interface were later combined by the IEC (International Electrotechnical Commission) to produce the IEC 958 standard.

The essential difference between the professional and the S/PDIF standard is not in the coding method of the analogue signal but in the format of additional data sent in the channel status block (see later). The frame structure and audio data coding are identical in both standards.

Subframes

The signal format of an IEC-958-interface consists of subframes, frames and blocks. Each sample of the audio signal is transmitted in a 32-bit subframe. The first four bits of the subframe form the preamble. Three types of preamble are possible, type B indicates that the sampled value in the subframe is for channel A (left) and is the first frame of a new 192 frame data block. Type M indicates left channel data also but this time it is not the start of the block. Type W indicates that the sampled value is for channel B (right).

The next 24 bits contains the digital code representing the sampled audio signal. The sampled value can be 24 bits long or less. CD players use 16 bit samples so the unused preceding bits will always be filled with zeroes. After this data sample a single validity bit is sent, if this bit is set it indicates that a sampling error was detected and the sampled value should be discarded. The next bit is 'user data' and conveys information (together with the other 'user data' bits in each of the subframes in a block). The information conveyed here could be for example text. Next comes the 'channel status' bit. Again each subframe contains a single channel status bit and these bits are used together in each block. These channel status bits contain information on the data channel and would include sampling rate, audio or data mode and professional or consumer mode. A parity bit is included as the last bit in the subframe and allows single bit transmission errors to be detected. Interpolation enables corrupted subframes to be simply discarded.

Frames and Blocks

Each frame contains as many subframes as there are audio channels. A standard stereo signal has one frame containing two subframes, one for the left and one for the right channel. The frames

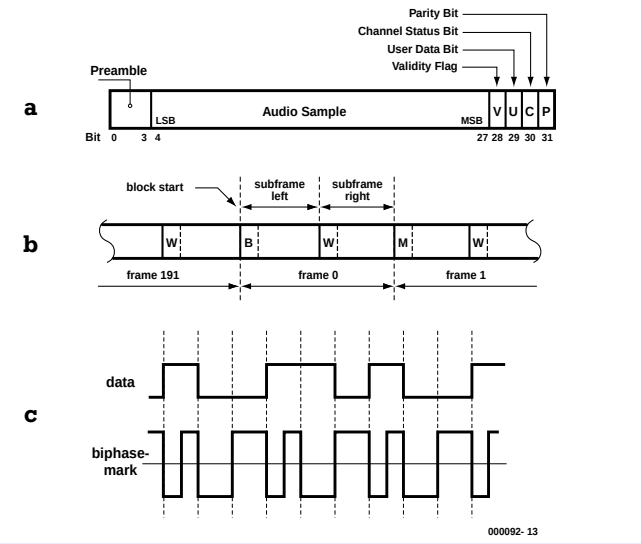

Figure 1. Data format of the S/PDIF signal.
a) A subframe
b) Frame and block format.
c) Biphase mark encoding.

are sent at the sampling rate so that for a CD player using a 44.1 kHz sample rate the data rate will be:

2 channels × 32 bits per subframe × 44.1 kHz = 2.8224 Mbit/s

192 frames make up a single block. The block structure allows 384 'user data' bits to be sent in one frame (one 'user bit' per subframe). In practice, the user bits in the left and right subframes are identical so that there is only 192 bits of information sent per block. The same is true for the 'channel status' bits.

Sending the B preamble in the first subframe ensures that the start of each block can be easily detected and the complete block can be correctly decoded. As we already mentioned, the structure of the channel status information differs for the professional and S/PDIF signals. The first bit indicates which of the two standards is used.

Biphase signals

At the physical level, the S/PDIF-interface uses a 75 Ω coaxial cable to convey the digital signal between equipment with Cinch connectors. The signal source equipment generates a 500 mVss signal level while at the receiving equipment a minimum sensitivity 200 mVss is necessary. Cable lengths in excess of 10 m are possible with this interface. The signal coding used is Biphase Mark Code (BMC) which is a sort of phase modulation. For every '1' in the data stream two zero crossing of the signal occur and for every '0' there is only a single zero crossing. The signal has no dc component so that ac coupling is allowed.

The professional IEC 958 interface has a signal level ten times higher than S/PDIF (3 to 10 V_{pp}), uses a balanced 110 Ω cable (twisted pair) and of course a different connector. Some form of coupling transformer is generally employed to reduce any earth loop problems.

input pin SPDIF of the UDA1350/1. The signal is amplified to CMOS levels and fed to the IEC 60958 decoder where a Phase Locked Loop (PLL) locks to the data and all the 24 bits of data for both left and right channels along with some key channel status bits are extracted from the bit stream. The signal now passes to the *Audio Feature Processor*, where in static mode de-emphasis for the IEC 60958 data stream is inserted. De-emphasis reduces the signal levels at the high frequency end of the signal spectrum which has the effect of also suppressing noise and so improving the signal to noise ratio. The de-emphasis simply compensates for the pre-emphasis that was added by the preced-

ing equipment (CD, DAT source etc). The net effect on the signal should be zero but with an improved S/N ratio. Next the *interpolator* converts the incoming data stream from $1f_s$ to $128f_s$ (where f_s is the sampling frequency) by cascading a recursive filter and a FIR filter. These filters introduce 50 dB attenuation to all of the signal components above about half of the sampling frequency. The *Noise Shaper* operates at $128f_s$. It shifts all of the in-band quantization noise up to frequencies beyond the audio band (10 Hz to 25 kHz). This ensures that a high signal to noise ratio is achieved. The noise shaper output signal is now converted into analogue by Filter Stream Digital to Analogue Converters (FSDAC). These are basically semi-digital reconstruction filters that convert the digital 1-bit data stream into analogue output signals. No additional external filters are necessary and the output signal swing is sufficient to drive a standard line input of an amplifier or a stereo headphone set.

The IEC 958 decoder strips off the left and right 24 bit long audio samples from the incoming data stream and also reads the channel status bits. These bits contain information on the pre-emphasis setting, the audio sampling frequency, the type of two channel Pulse Code Modulation (PCM) coding and the clock accuracy detection. An internal phase locked loop (PLL) enables the system to lock onto signals with the sample rates of between 28 kHz and 54 kHz. This range includes the most common sample rates of 32 kHz, 44.1 kHz and 48 kHz. Swapping the UDA1350ATS with the pin compatible UDA1351TS will enable the circuit to use sample rates up to 100 kHz.

LED D1 indicates that the IEC 958 decoder has locked onto and recognised the input data stream. When the code is not recognised D1 will be off and the audio output is muted. **Table 2** shows the common sampling rates together with the corresponding data rates and indicates the suitability of the UDA1350ATS or UDA1351TS.

Table 2.

Sample rate and corresponding data rate.

UDA1351TS	UDA1350ATS	Sample rate	Data rate
X	X	32.0 kHz	2.048 Mbit/s
X	X	44.1 kHz	2.8224 Mbit/s
X	X	48.0 kHz	3.072 Mbit/s
X		64.0 kHz	4.096 Mbit/s
X		88.2 kHz	5.6448 Mbit/s
X		96.0 kHz	6.144 Mbit/s

The circuit

The complete circuit shown in **Figure 2** consumes approximately 10 mA quiescent current (with no digital input signal) and less than 30 mA operational. An LM317 voltage regulator (IC2) is used to produce the 3.0 V supply from a 9 V battery.

As we saw earlier IC1 contains several circuit blocks that together perform all the functions of the chip. All of these analogue and digital circuits together on the same chip can give rise to interference and crosstalk especially on the supply voltage. To reduce the possibility of this the IC is manufactured with separate pins for supply voltage to the different

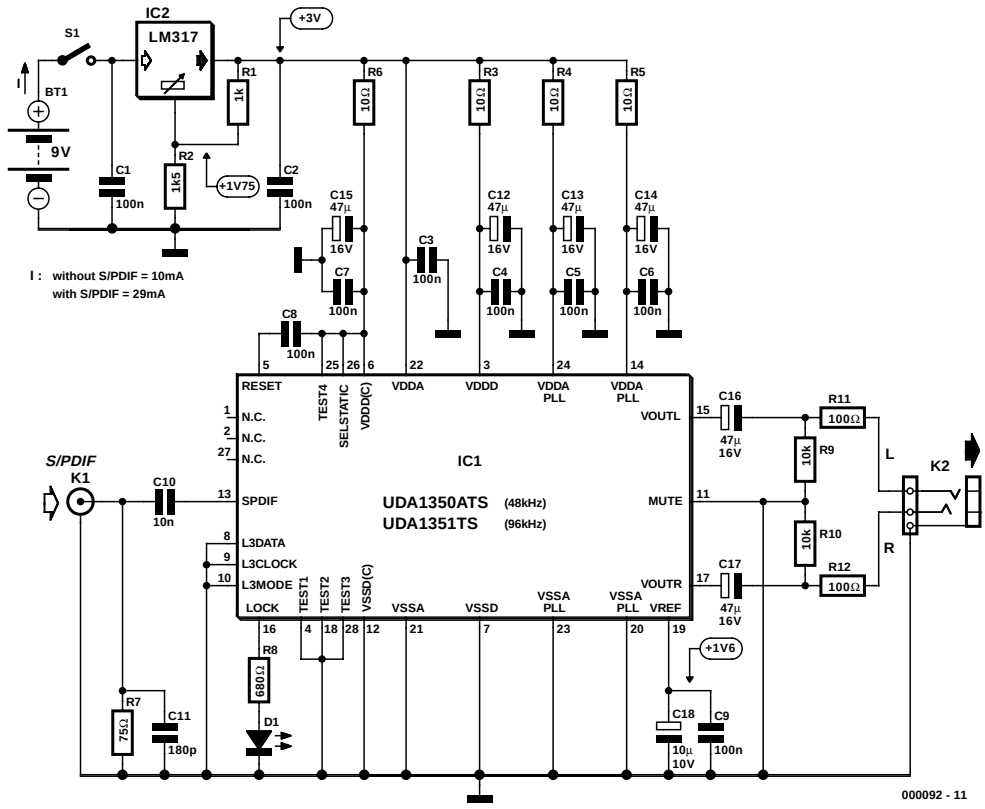

Figure 2. Circuit diagram of the S/PDIF checker

stages. A 10 Ω resistor together with a 47 µF and 100 nF capacitor form a network at each of these supply voltage input pins to ensure minimum interference. Capacitor C8 generates an active high RESET signal when the chip is powered up. The internally generated reference voltage level used by the D/A converters is half of the supply voltage level and is brought out to pin 19 where capacitors C18 and C9 are used to store and smooth VREF.

The COAX cable connecting the digital signal to the input of the test unit has an impedance of 75 Ω. Resistor R7 is used to match the cable impedance with the unit's input impedance and reduce any reflections that would otherwise occur. The level of the digital input signal should be +0.2 V to +3.3 V peak-to-peak and is ac-coupled to the input of IC1 by capacitor C10.

The LOCK output signal from IC1 is generated by the in-built IEC958 decoder and will only be high when a valid PCM audio signal is detected. LED D1 will therefore give a good indication that the input signal is in order. The active-high MUTE input (pin 11) is not used in this application so it is tied low to ensure the output will not be muted. Any valid digital input signal will always be available as analogue signals at the outputs unless the input signal is corrupted or of the incorrect format in this case an internal circuit will mute the output to prevent the noise burst that would otherwise be audible.

Both audio outputs from IC1 are ac-coupled with 47 µF capacitors (C16 and C17) to the output socket K2. The 10 kΩ resistors ensure that the output signals have a load when there are no headphones connected. The 100 Ω series resistors provide output short-circuit protection.

Building and testing

Both the UDA1350ATS and the UDA1351TS are supplied in an SSOP28 package (Shrink Small Outline Package with 28 pins). There is no ready-made PCB available for the design but in this case it is not too much of a disadvantage. Apart from the main chip there is very little external circuitry so the entire circuit can be contained on a small piece of SMD prototyping board. Begin building the circuit by fitting the voltage regulator chip IC2 together with RI, R2, C1 and C2. Before any other components are fitted check that 3.0 V is available at its output when a 9 V battery (or better still for test purposes a power supply with current limit set to 50 to 100 mA) is connected to the battery connector. If the voltage level is correct you can now turn off the power and solder IC1 in position along with all the remaining components. Next, using an eyeglass, check all the solder joints and especially the SMD connections for any unintentional solder bridges that you may have made. If you are confident that all is in order, power the circuit up, plug in some headphones to connector K2 and connect a digital audio signal to connector K1. If there is no audio output check the supply voltage again at all the points where it enters IC1 and also check that VREF is at 1.6 V (pin 19 on IC1). Any level that is less than it should be indicates that there is probably a solder bridge causing a short-circuit somewhere so power down, take up the eyeglass and look again. If all the voltages are OK and still nothing can be heard try connecting a different digital signal at the input. (000092-1)